RISC-V Opt-VP:
An Application Analysis Platform Using Bounded Execution Trees

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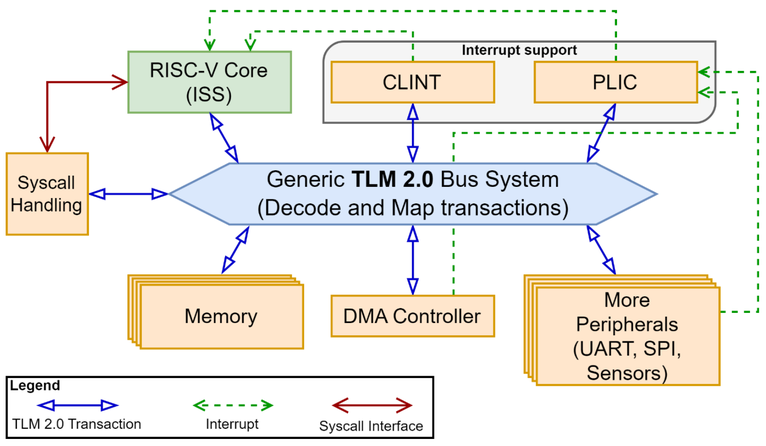
1. Overview

- **Tailoring hardware** to applications significantly increases their performance.
- **Virtual Prototypes** (VPs) enable early software development and design space exploration
- **RISC-V Opt-VP** is a Virtual Prototype driven binary analysis platform
- By analyzing the execution, it identifies **instruction sequences** that are promising candidates for hardware optimization

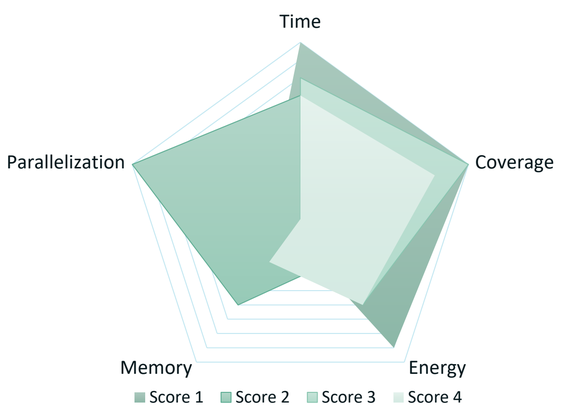
2. Virtual Prototype Driven Tracing

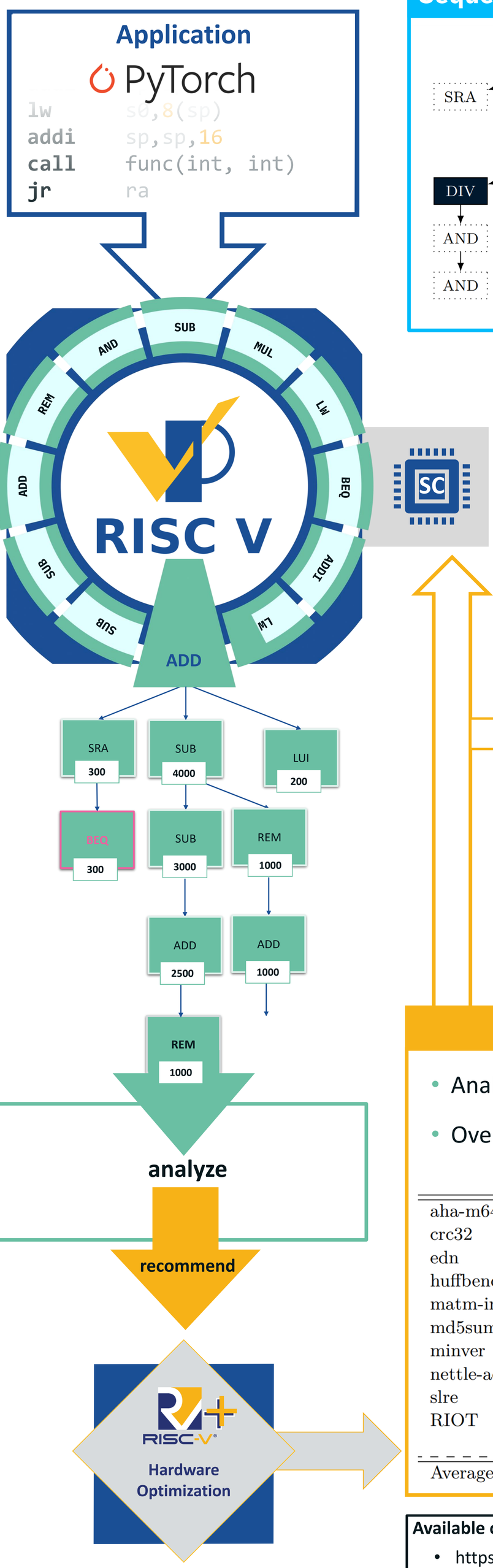
- Extend RISC-V **Virtual Prototype**
- Tracing module interfacing ISS core
- Construct **bounded execution trees**
- Lossless compression of trace information
- Identify promising hardware optimization candidates based on recurring patterns



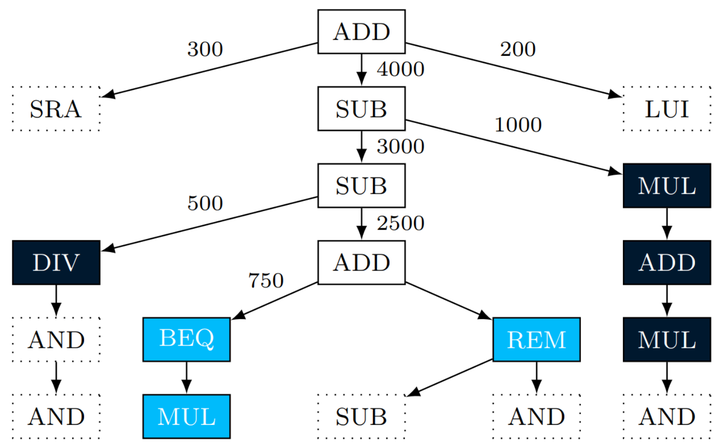
3. Analysis

- Analyze trees using a **scoring function**
- Choose a set of **metrics** that matches the target hardware optimization
- E.g. $Score(Seq) = weight_{Seq} \cdot |Instructions|$





Sequence Merging



VP Extension

- Extend VP to include new optimization
- E.g. via communication over SystemC bus
- Iterate analysis and design

ASIC/FPGA

- Implement accelerator on FPGA
- Evaluate performance gain
- Update VP to improve analysis and performance estimation

4. VP Evaluation

- Analyze Embench and RIOT
- Over 30% expected coverage on average

	Root	Len	Weight	Total #	NP
aha-m64	SRLI	11	162432	4532K	185.0
crc32	JAL	12	175104	3846K	71.5
edn	LH	5	290400	3483K	104.2
huffbench	ADDI	1	661440	2515K	1
matm-int	ADD	5	357200	4426K	80.7
md5sum	SLLI	24	39936	2339K	105.3
minver	SW	5	100114	2818K	88.8
nettle-aes	LW	31	32864	4481K	99.7
slre	SW	7	107007	2570K	204.0
RIOT	ADDI	1	3893	13K	1
Average	-	6.52	339986	30.95%	59.76

Available on GitHub:

- https://github.com/agra-uni-bremen/opt-vp
- https://github.com/agra-uni-bremen/opt-seq

Funded by:

Federal Ministry of Education and Research

ECXL FAIRe Scale4Edge

Grant number 16ME0127, 01IW22002 and 01IS23074

Read the extended abstract:

Universität Bremen

dfki ai Deutsches Forschungszentrum für Künstliche Intelligenz
German Research Center for Artificial Intelligence