Karlsruhe Institute of Technology

Institute for Data Processing and Electronics (IPE)
ASIC and Detector Laboratory (ADL)

Silicon Implementation of a RISC-V Processor for the AstroPix Multi-Channel Readout Controller

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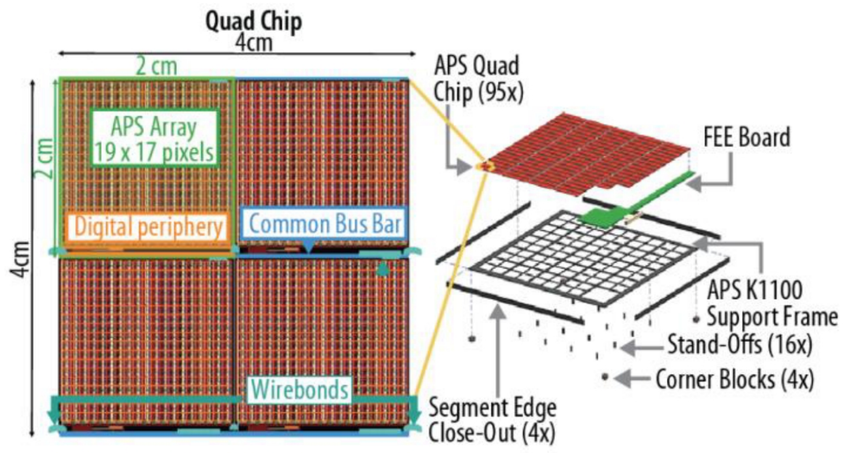
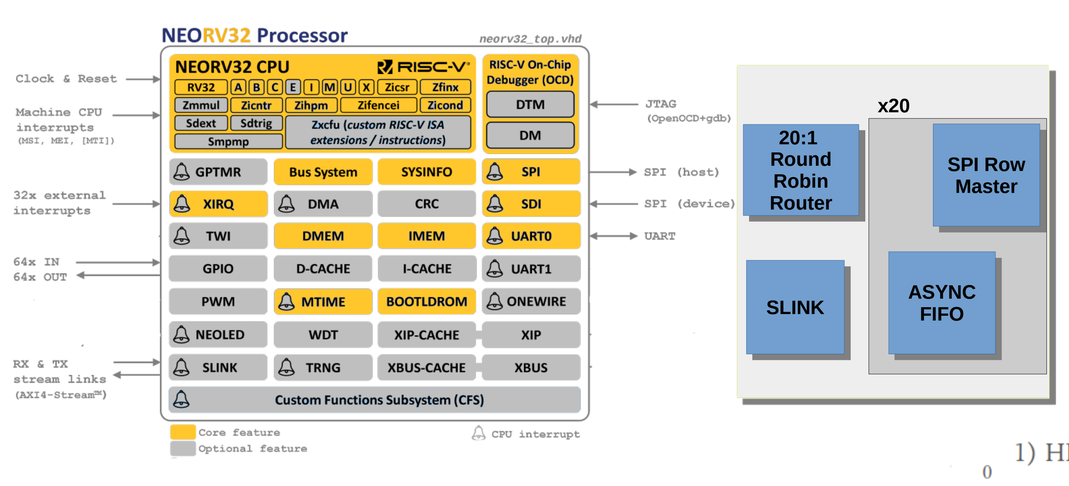
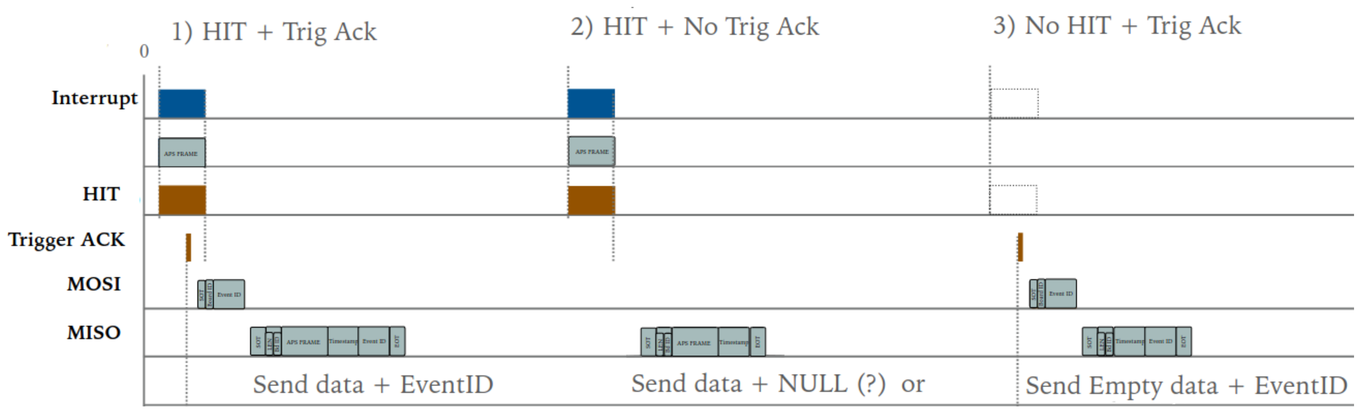
- **Substitute costly FPGA** based Data Processing
- Investigate instead **ASIC implementation** of a soft-core RISC-V based Microcontroller in a 110 nm UMC process as part of a **low power** readout of an entire AstroPix sensor system layer
- AstroPix is HV-CMOS a silicon tracker sensor for astro-particle experiments
- Matrix of AstroPix as part of a Gamma-ray space based Observatory (AMEGO-X)

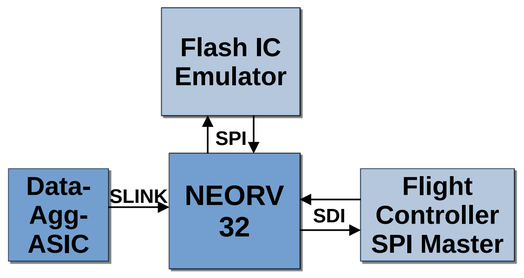




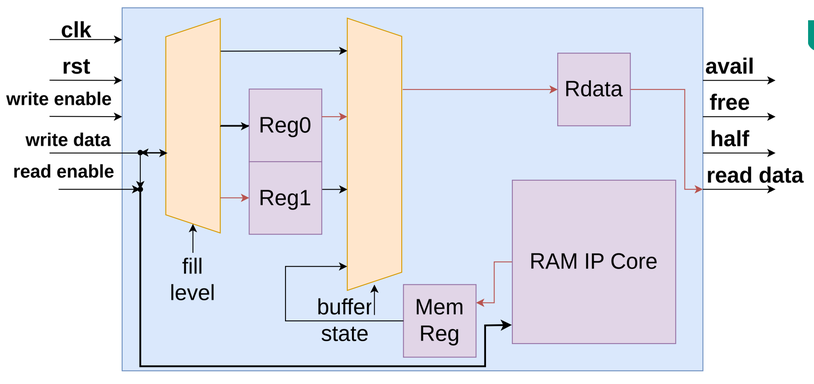
- 2 Main Modules:
  - Open-source **32-bit NEORV32 Processor**
  - Data aggregator ASIC interfaced via AXI
- NEORV32 has extensive configuration options and documentation to design for application requirements

- **Simulation Testbench Setup** to define required I/O Modules and 1st configuration of the Processor ASIC
- Includes a Test Application Software with **3 different data packages** based a on simple protocol
- **Application stored inside ext. Flash RAM** module and loaded via SPI with internal Bootloader





- **Next Steps**: After finished RTL Design, Gate Netlist Synthesis
- Floorplanning, Place&Route, Clock Design



- **Adapt RTL Memory Design** of NEORV32 based on RAM IP Cores
  - Own synchronous and asynchronous First Word Fall Through FIFOs
  - Own Instruction Memory and Data Memory
- Implement **mitigation** Strategies for **radiation hardness**, more thorough **Validation** of the entire design, **Data aggregator ASIC design**

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