eduBOS5: RISC-V uController Dev Experience

From Combo to Pipelined, optimising PPA metrics for FPGA

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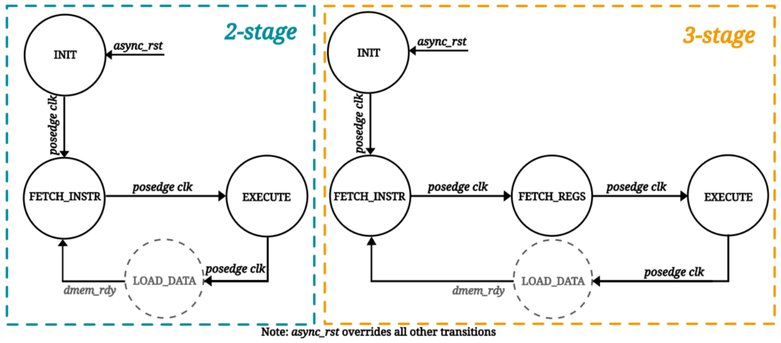
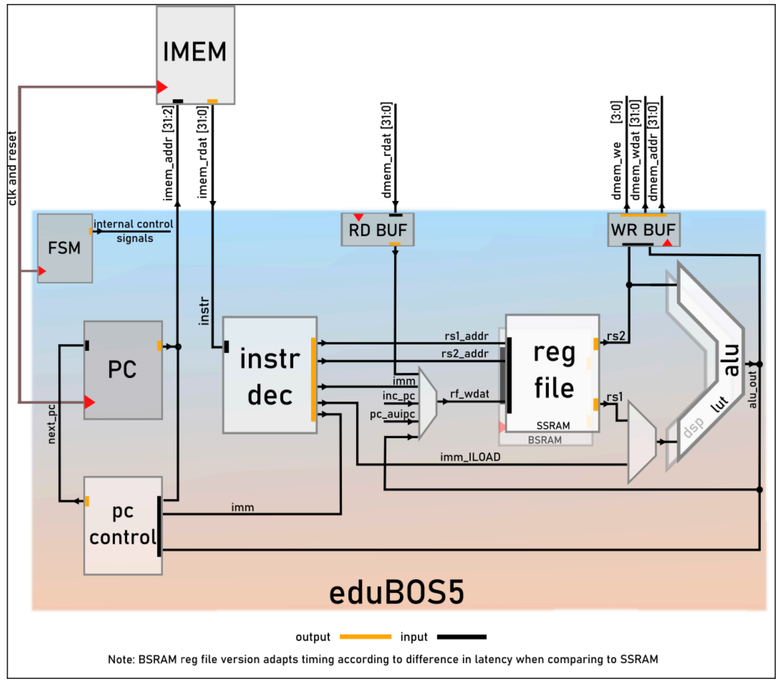
Introduction

- Soft configurable RISC-V micro-controller, custom-tailored for FPGAs. High on compute throughput, low on everything else.
- Single-threaded M privilege implementation of RV32I RISC-V ISA.
- For Gowin, Xilinx, LatticeSemi and CologneChip.
- For best results, use proprietary Synth and PNR.
- Verification flow, including QA and linting, is based on open-source tools.
- Two simulation options: (1) Cycle-accurate, all-RTL testbench; (2) Fast, ISS-based HW/SW co-sim, by tapping into Vproc technology.
- Many add-ons for DSP and AI workloads.
- Primarily for bare-metal apps. FreeRTOS option.

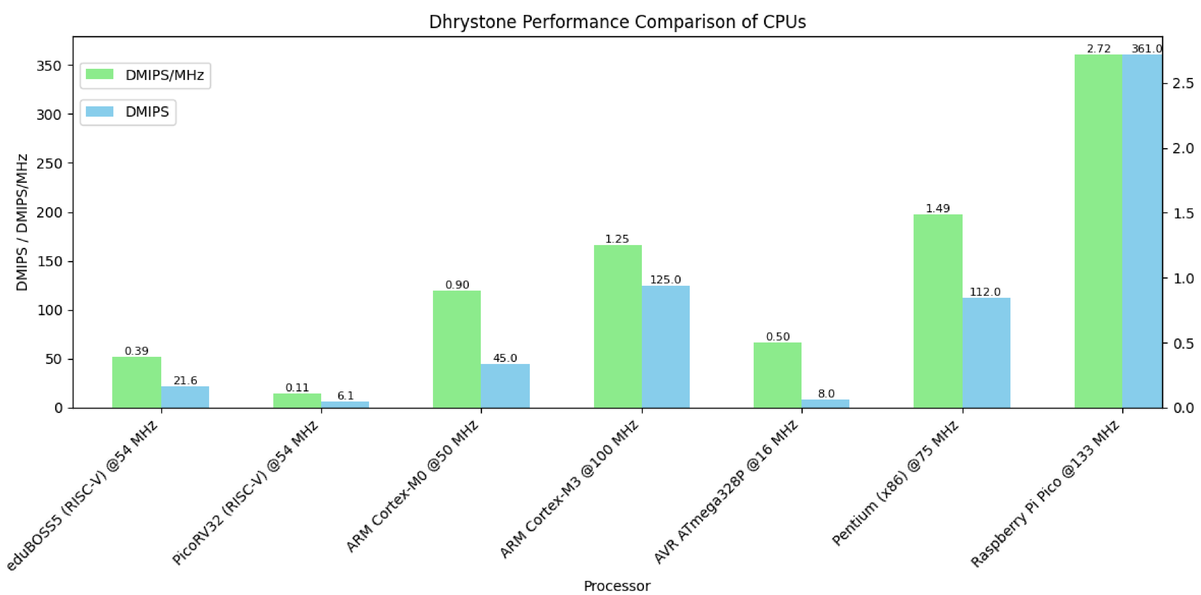
Design Overview

- Harvard architecture with 2 or 3 stage pipeline.
- Pipelined data bus isolates it from SOC growth.
- ALU can be in either generic LUTs or DSP HM.
- RF can be in either LUTRAM or BlockRAM.
- Fluid internal pipeline stages accommodate latencies differencies of all these combinations.
- RTL is written in clean SystemVerilog-2017.





Performance comps with PicoRV32 and up



PPA comps for impl options and FPGA targets

- CPI = 2.56
- Area = cca 1000 Gowin LUTs + 400 FFs
- Fmax = 80-100MHz
- DMIPS/MHz = 0.39 (Dhrystone)

Vendor	Tools	Chip	Implementation	Fmax (MHz)	LUT	FF	Distributed RAM	BSRAM	DSP	DMIPS/MHz	DMIPS	Pnor
Xilinx	Vivado v2024.1	Artix-7 XC7A35T-ICPG236C	*PicoRV32 (SSRAM RF, LUT_ALU)*	193.000	966	424	48	-	-	0.112	21.616	8.625
			eduBOS5 (SSRAM RF, LUT_ALU) - 2stage	130.500	810	450	48	-	-	0.39	50.895	2.077
Lattice	Lattice Diamond	ECP5 LF5U-12F-6BG381C	*PicoRV32 (SSRAM RF, LUT_ALU)*	94.060	1013	428	96	-	-	0.112	10.534	9.045
			eduBOS5 (SSRAM RF, LUT_ALU)	71.669	929	458	96	-	-	0.39	27.951	2.382
Gowin	Gowin FPGA Designer 1.9.9.03	GW2AR-18C C8/I7	*PicoRV32 (SSRAM RF, LUT_ALU)*	118.316	1340	414	32	-	-	0.112	13.251	11.96
			eduBOS5 (SSRAM RF, LUT_ALU) - 2stage	88.081	1022	450	32	-	-	0.39	34.340	2.621
			PicoRV32 (SSRAM RF, DSP_ALU) N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
			eduBOS5 (SSRAM RF, DSP_ALU) - 2stage	113.610	902	385	32	-	2	0.39	44.308	2.313
			PicoRV32 (BSRAM RF, LUT_ALU)	116.327	1353	458	-	2 (32 kbits)	-	0.112	13.029	12.08
			eduBOS5 pipelined (BSRAM RF, LUT_ALU) WIP, forecasted:	70.000	1000	450	-	1 (16 kbits)	-	0.8	56.000	1.250
		GW1NR-9C C6/I5	*PicoRV32 (SSRAM RF, LUT_ALU)*	63.324	1340	414	32	-	-	0.112	7.092	11.96
			eduBOS5 (SSRAM RF, LUT_ALU) - 2stage	50.819	1022	450	32	-	-	0.39	19.819	2.621
			PicoRV32 (SSRAM RF, DSP_ALU) N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
			eduBOS5 (SSRAM RF, DSP_ALU) - 2stage	56.052	902	385	32	-	2	0.39	21.860	2.313
			PicoRV32 (BSRAM RF, LUT_ALU)	55.815	1353	458	-	2 (32 kbits)	-	0.112	6.251	12.08

https://github.com/tarik-ibrahimovic/eduBOS5