To Clock or not to Clock: Clock Gate Insertion with a Yosys-based Netlist Modification Tool

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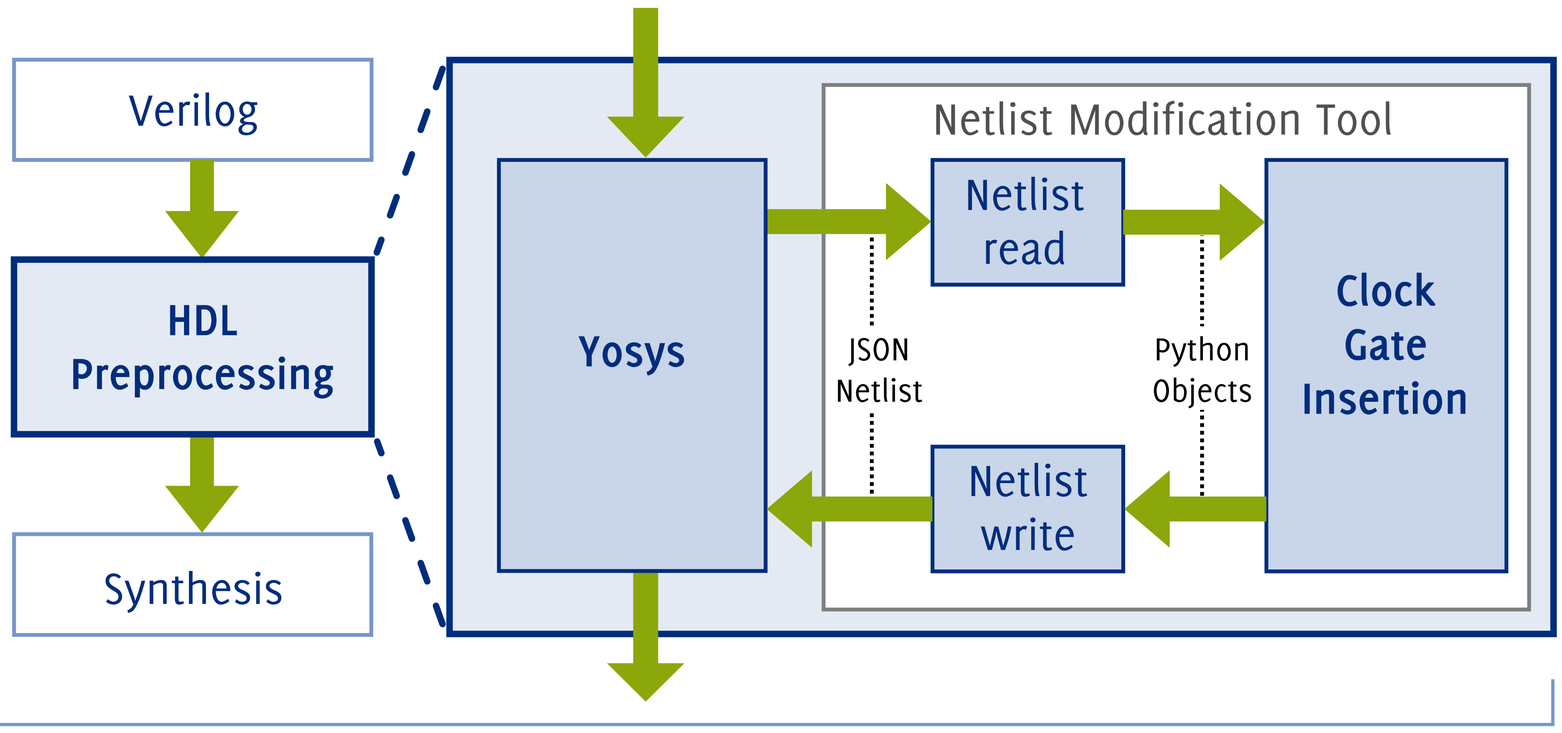
Motivation

- Energy reduction is an important challenge in the design of intelligent systems
- The less energy the system consumes, the less demand there is on the power supply
- **Clock Gating** is a common method in digital circuits to prevent unused logic from consuming power [1]

Workflow for Clock-Gate Integration

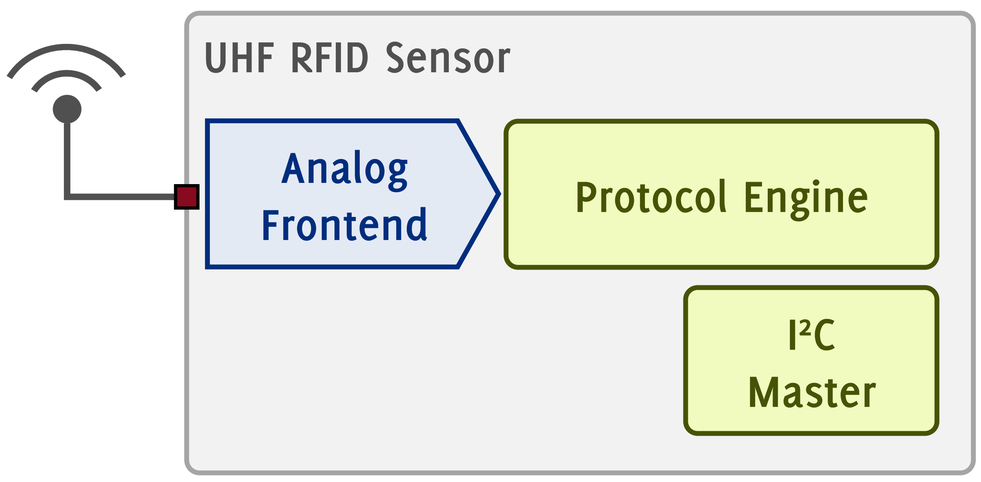
- Import design files to Yosys
- Yosys transforms design into internal representation using generic gates
- Export Yosys representation to JSON format, search for FFs and insert clock gates
- Import updated representation into Yosys and create design netlist from standard cell gates
- Run LEC to verify that changes have not altered functionality



Case Study: Protocol Engine for a UHF RFID to I²C Bridge

Device Under Test

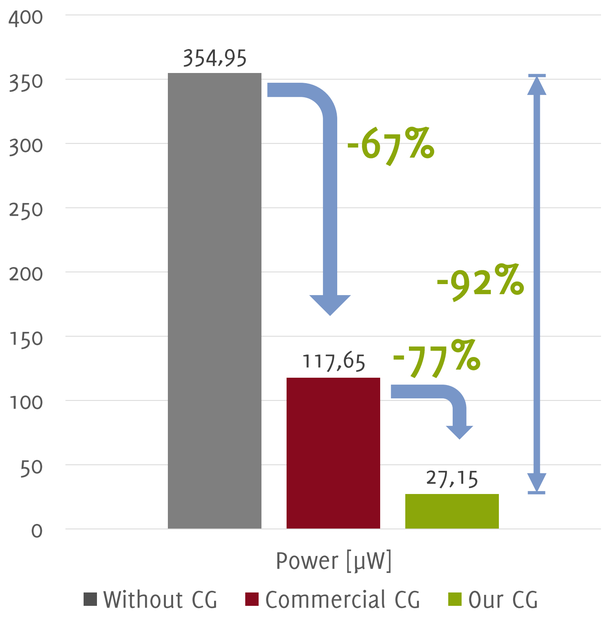
- Current UHF RFID sensor system consumes high amounts of power
- Sensor system is inactive when no request from reader is received
- Applying clock gating can achieve high yield in power reduction
- Simulation of revised chip layout with our clock gating and power consumption analyzation

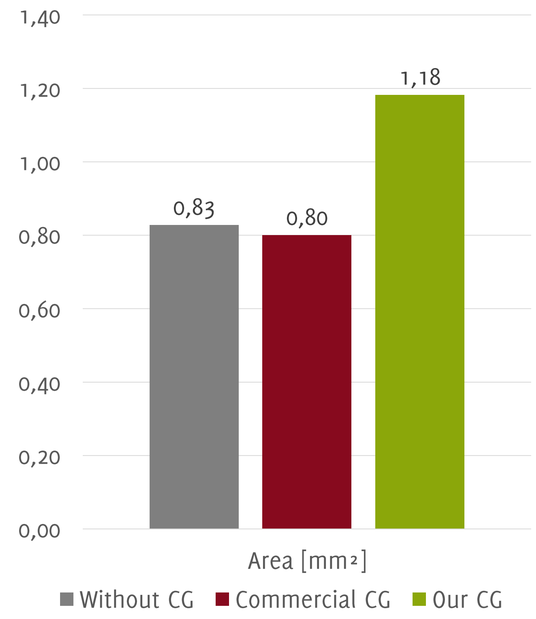


Digital backend consists of protocol engine for handling UHF RFID communications and programmable I²C controller

Power Estimation for Post-Route Test

- Simulate communications between reader and tag
- Reader sends command to select the tag for next query
- Activity profile of communications generated by Cadence Xcelium tool
- Power is estimated using static power analysis from Cadence Genus tool





- Our method reduces power consumption by the factor of ≈4 compared to commercial tools
- Comes with the cost of doubling the gate count (but only 30 – 50% area increase)

Roadmap

Present	Application	Further Developments	Future Goal
– Insertion of clock gates – Insertion of coverage monitors [2]	– Workflow applied to chip designs for power reduction or coverage extraction	– Open-Source EDA tools in the Meta-X Project – Open-Source Python-Tool	– One-click EDA tool solutions – Advanced power consumption reduction

[1] G. Gläser, et. al., "From Low-Power to No-Power: Adaptive Clocking for Event-Driven Systems," Forum on Specification & Design Languages (FDL) 2018, doi: 10.1109/FDL.2018.8524131
[2] M. Jirsak, et. al., "Under Cover: On-FPGA Coverage Monitoring by Netlist Instrumentation," SMACD Conference 2023, doi: 10.1109/SMACD58065.2023.10192205

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