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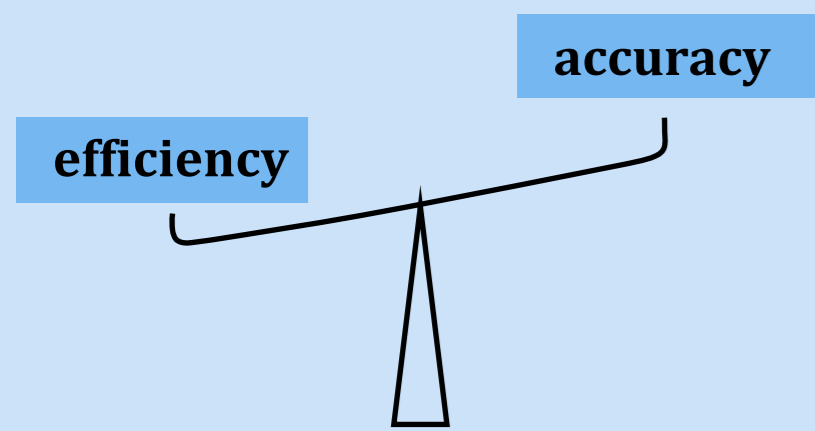
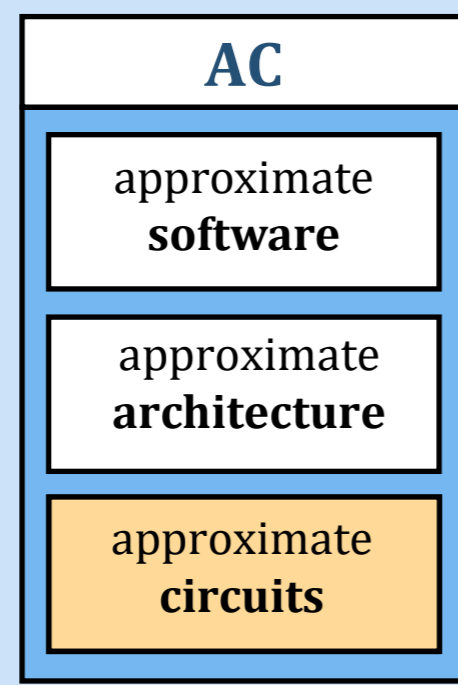
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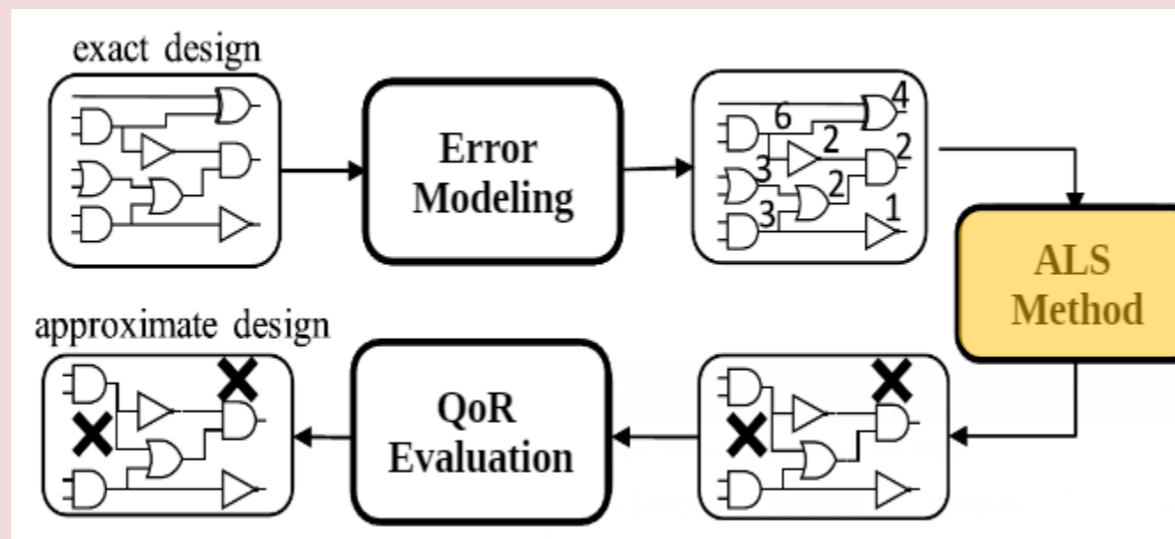
APPROXIMATE COMPUTING

An emerging design paradigm that exploits **error resilience** to obtain **efficient implementations**, at the expense of a slight **reduction in the result quality**.

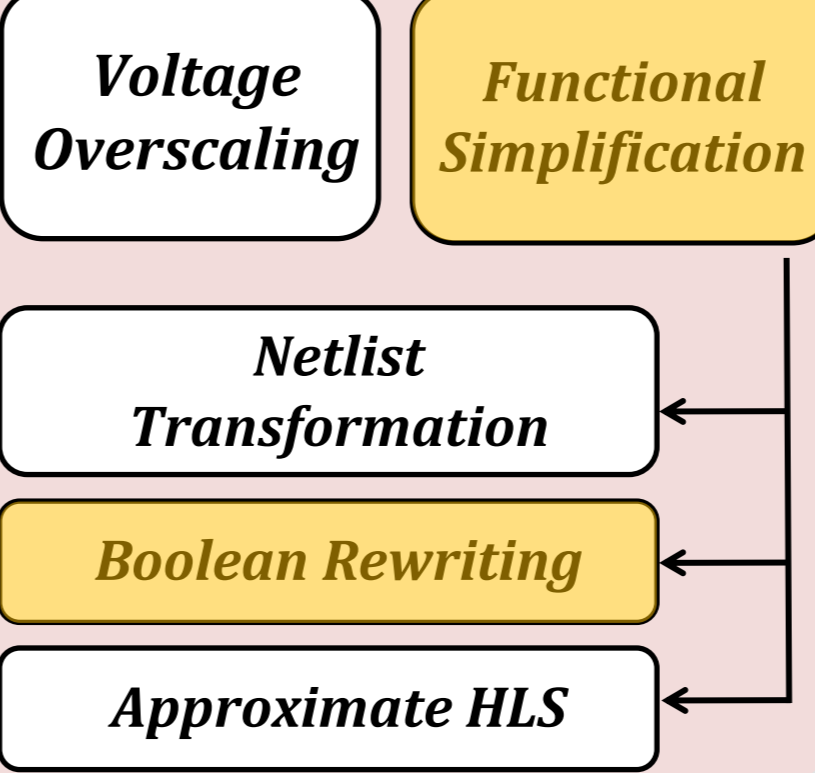


APPROXIMATE LOGIC SYNTHESIS

Typical ALS Flow



Approximate Circuits

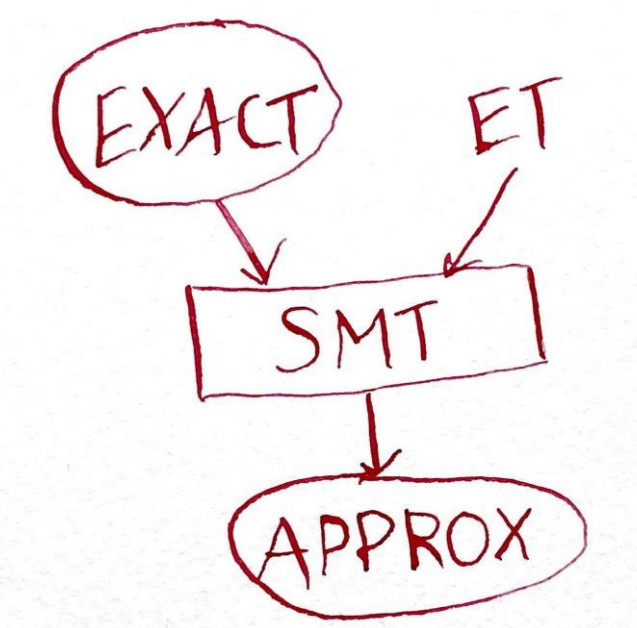


IDEA & TEMPLATE FORMULATION

Problem Formulation

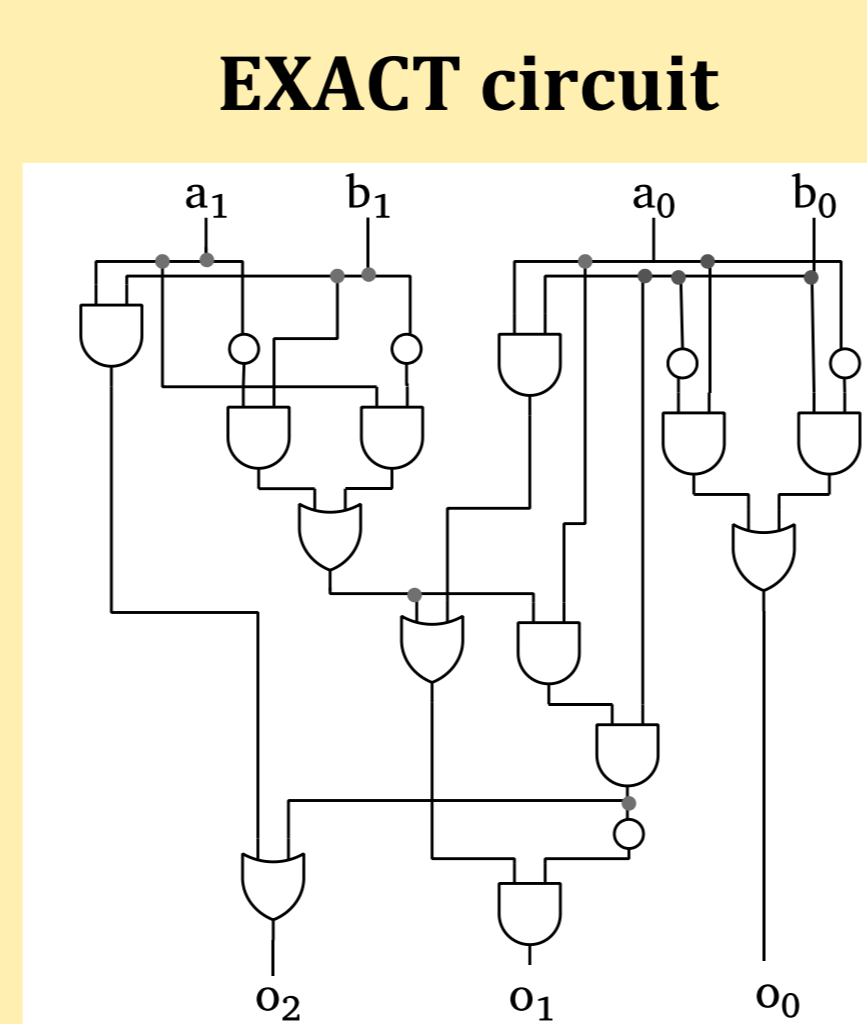
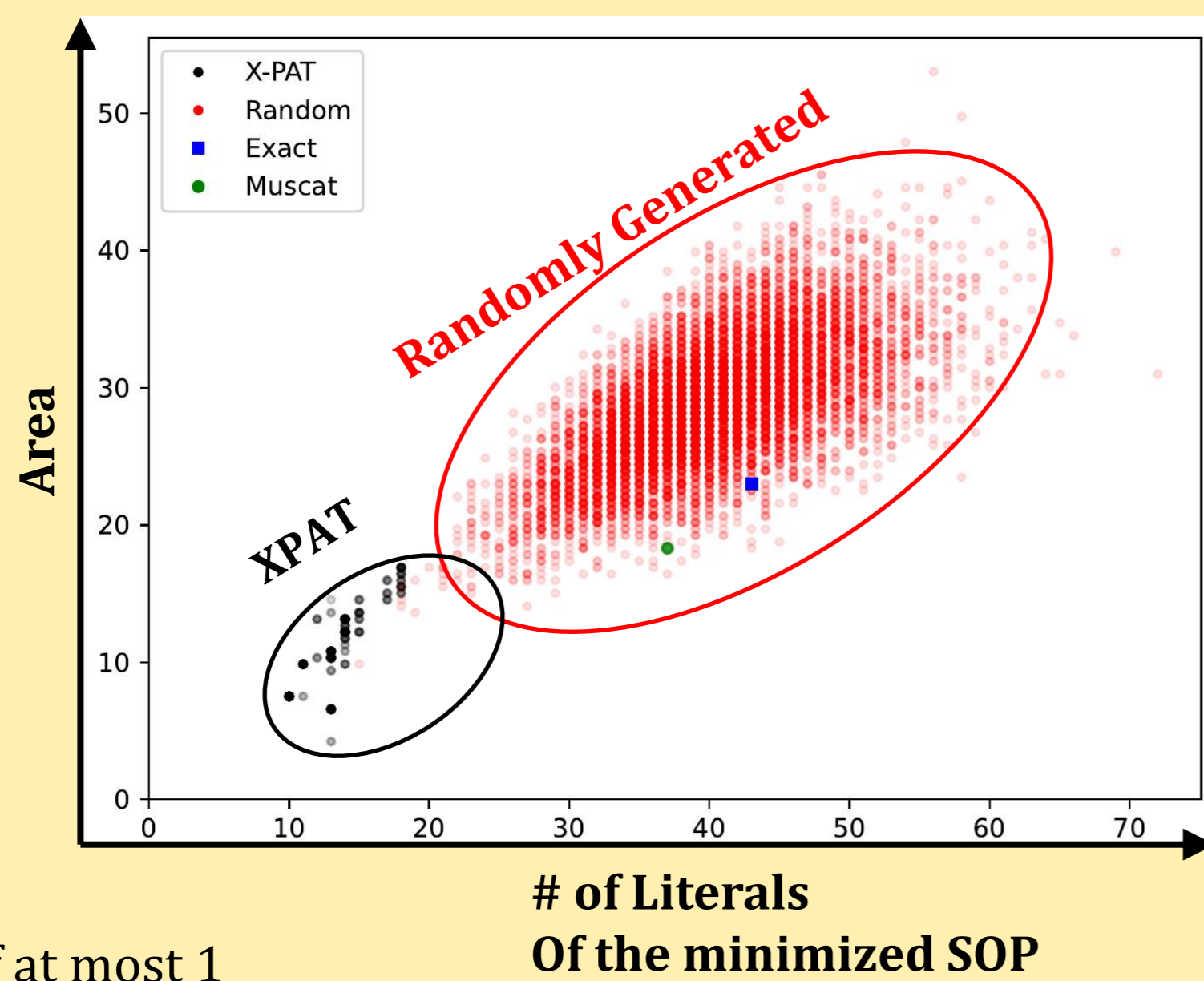
*Use an SMT solver to find/design the approximate circuit

*Given an EXACT circuit and error bound (ET) find approximate circuit (APPROX)

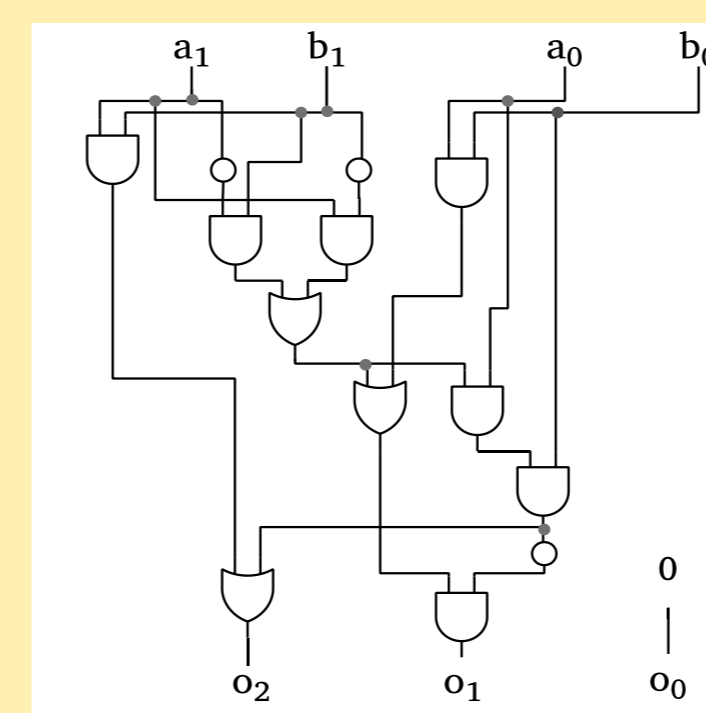


MOTIVATIONAL EXAMPLE

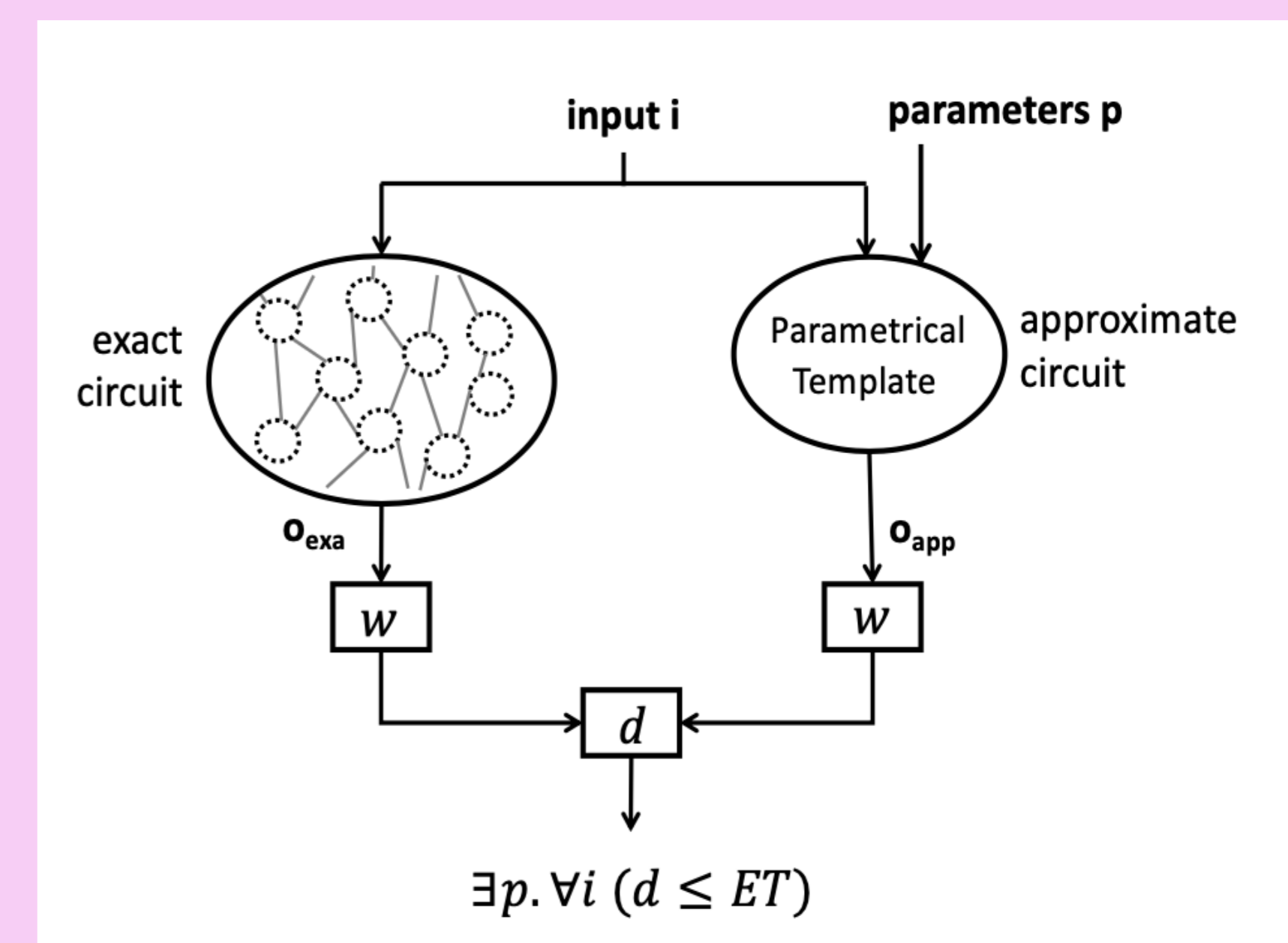
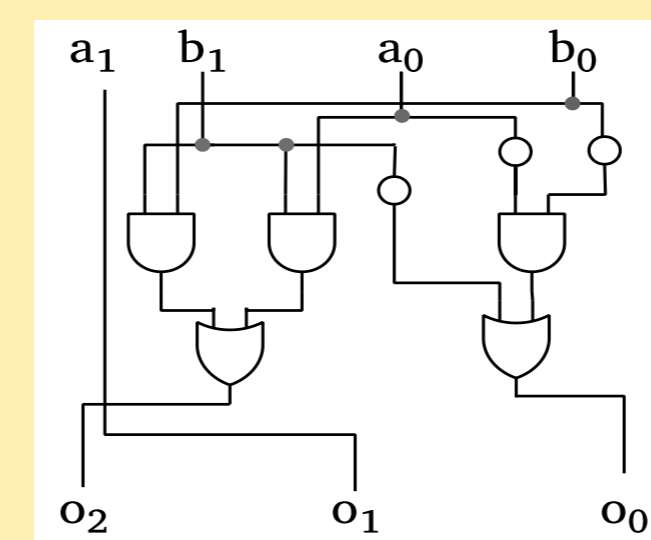
a + b	out	
0+0	0	Exact
0+1	1	Exact
0+2	2	Exact +1
0+3	3	Exact +1
1+0	1	Exact
1+1	2	Exact
1+2	3	Exact +1
1+3	4	Exact +1
2+0	2	Exact
2+1	3	Exact
2+2	4	Exact +1
2+3	5	Exact +1
3+0	3	Exact
3+1	4	Exact
3+2	5	Exact +1
3+3	6	Exact +1



MUSCAT circuit



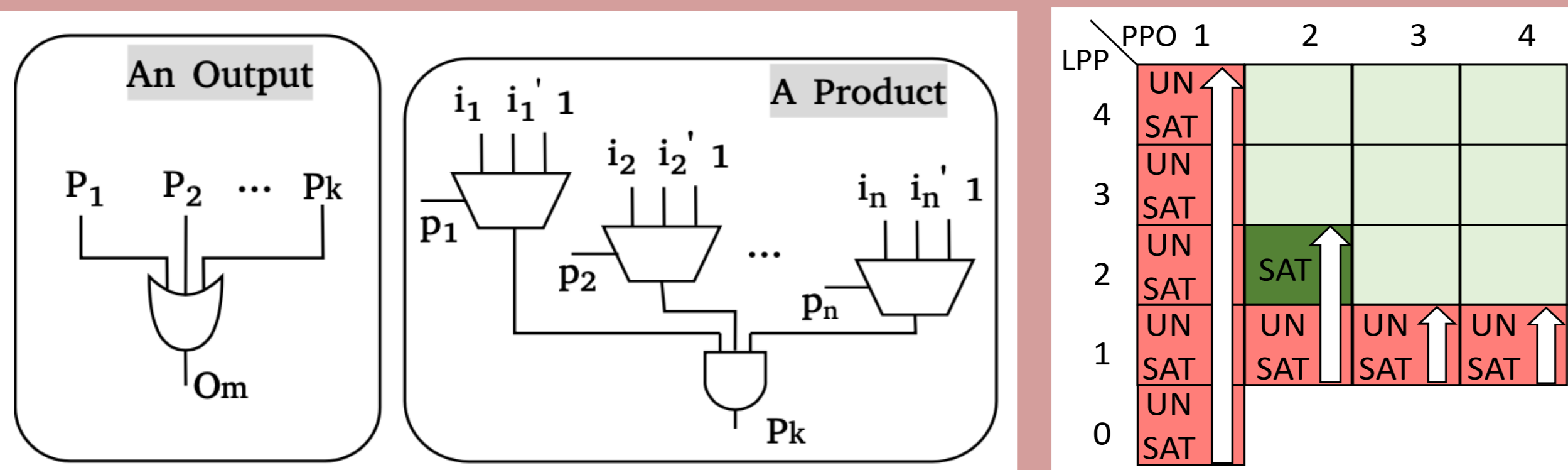
XPAT circuit



- If I can tolerate an error of at most 1
- $3^{16} = 22M$ different truth tables

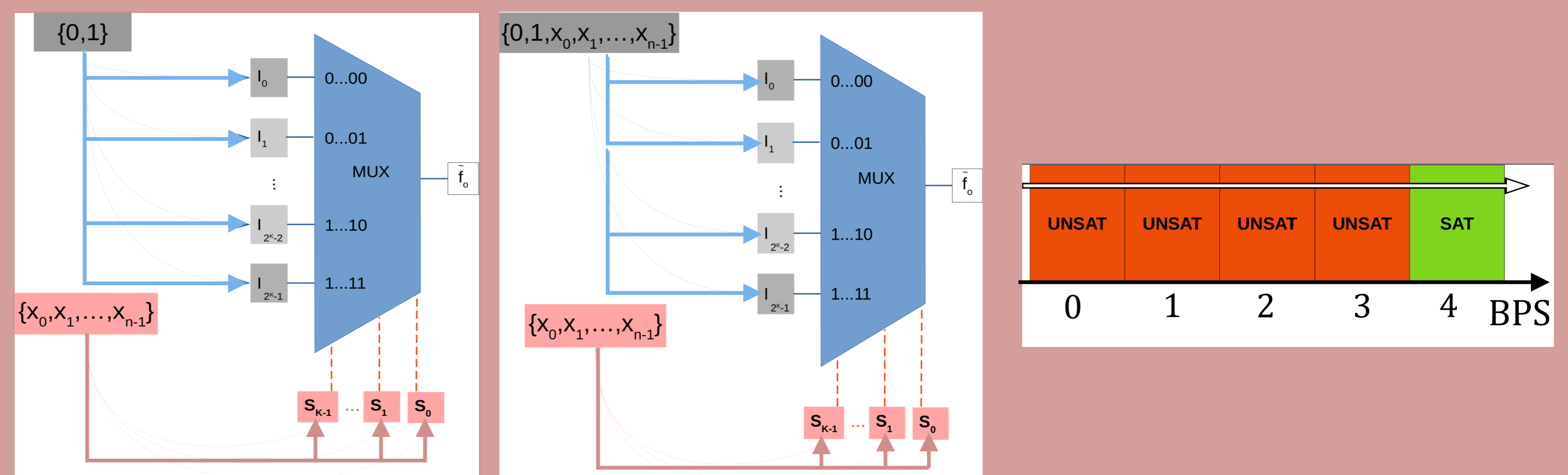
Contribution 1) ASIC SOP TEMPLATE (XPAT)

By limiting the number of Products Per Output (PPO),
And by limiting the number of Literals Per Product (LPP)
Smaller circuits can be found sooner



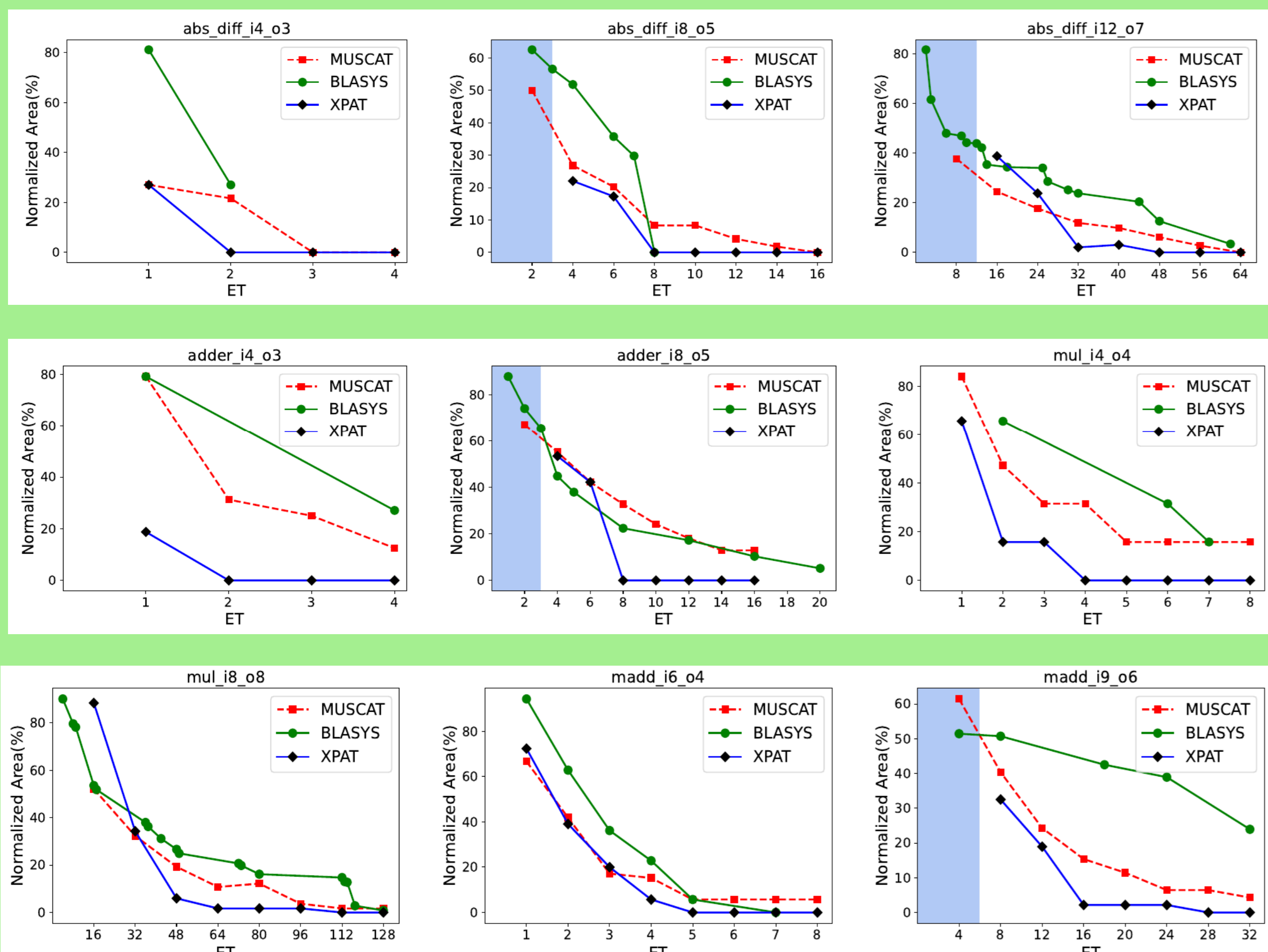
Contribution 2) FPGA LUT TEMPLATE

By limiting the number of Bits Per Selector (BPS)
Smaller circuits can be found sooner

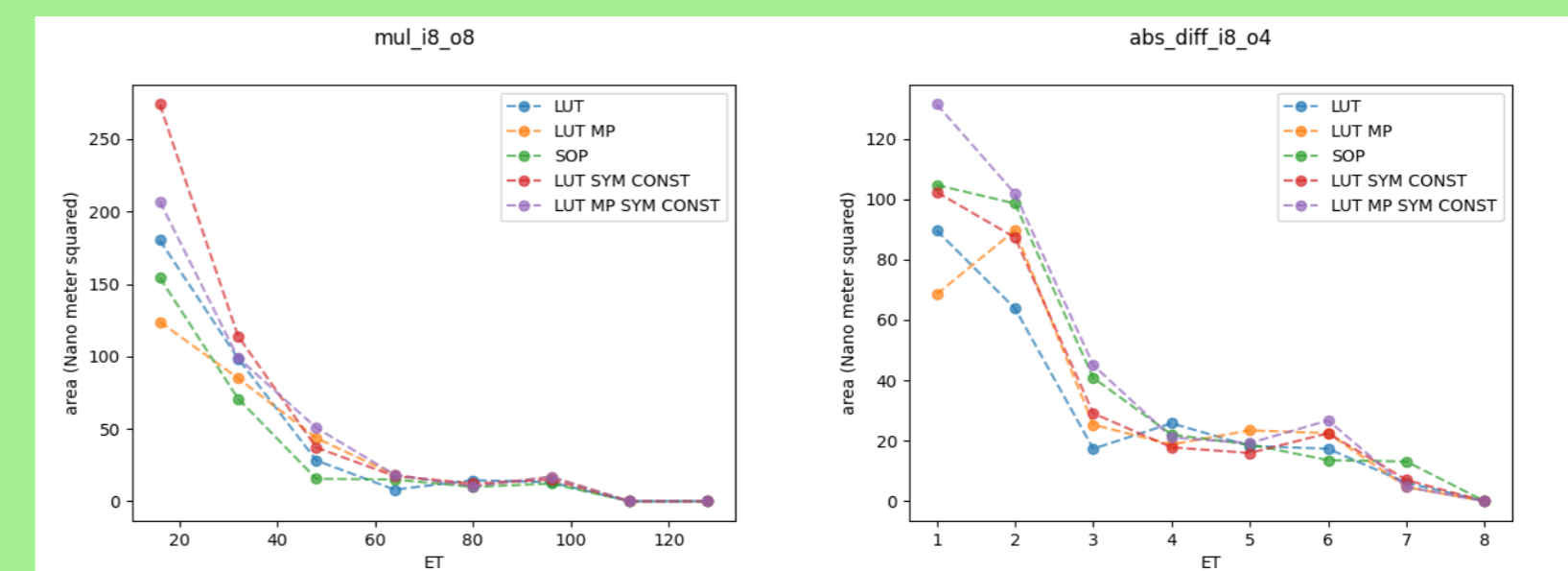


EXPERIMENTAL RESULTS

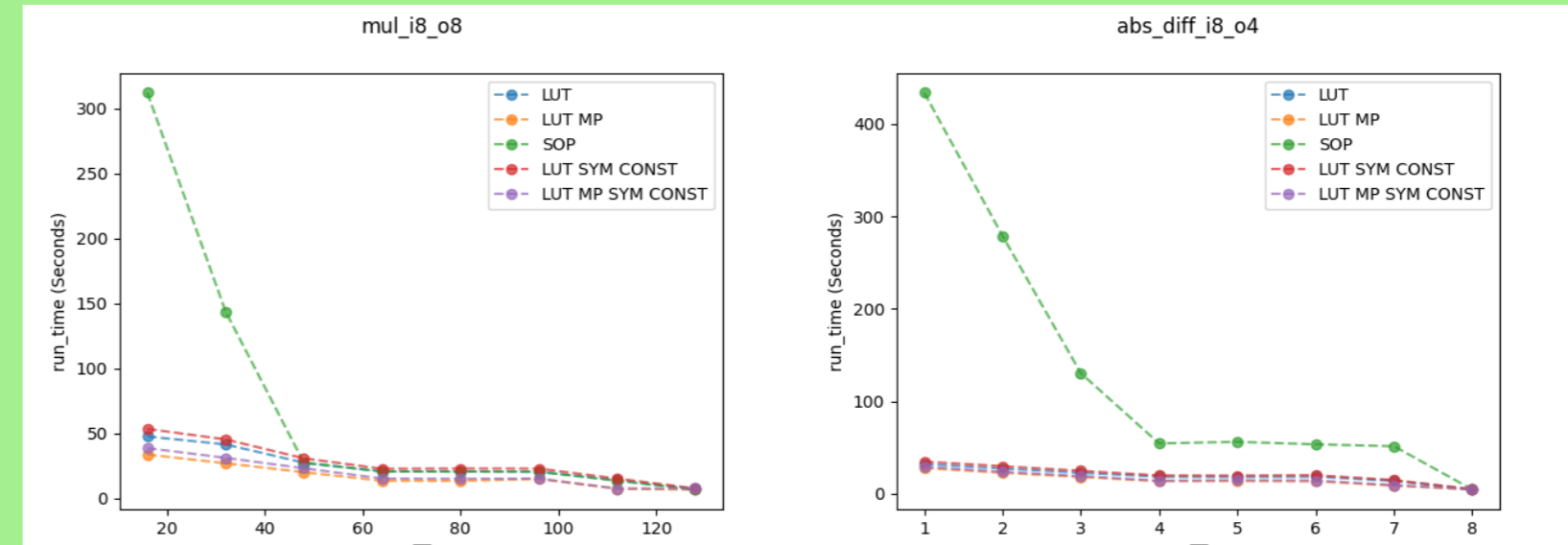
Area XPAT vs. state-of-the-art



Area XPAT vs. LUT



Runtime XPAT vs. LUT



- For the first time, employing an SMT solver (directly) to design the approximate circuit
- Innovative ALS technique based on Boolean rewriting of circuits according to a parametrical template
- Beats state of the art, albeit for small circuit so far
- Future work will consider hierarchical use of XPAT, and potentially the use of different templates