FPGA IGNITE Summer School 2024

Energy-Efficient Deep Learning Accelerators with Workload Awareness for Embedded FPGAs

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Motivation

Moving Intelligence to End Devices Offers Benefits

- Lower latency
- Higher accessibility
- Higher reliability
- Data security and privacy

System Model Targeting Energy-Efficiency

- Low-power MCU for coordination and networking
- Embedded FPGA for application-specific DL accelerators

Goal

"Combining efficient inference with workload awareness to optimizing DL accelerators for embedded FPGAs"

Requirements

- Support Various Architectures (MLPs, CNNs, RNNs,Transformers)
- Maintain Acceptable Model Precision Loss

Constraints

- Inference Time: Below the latency required by the application
- Energy: Within a fixed budget per inference
- Resource: Fit FPGA (such as XC7S15, ICE40UP5K)

LSTM Accelerators

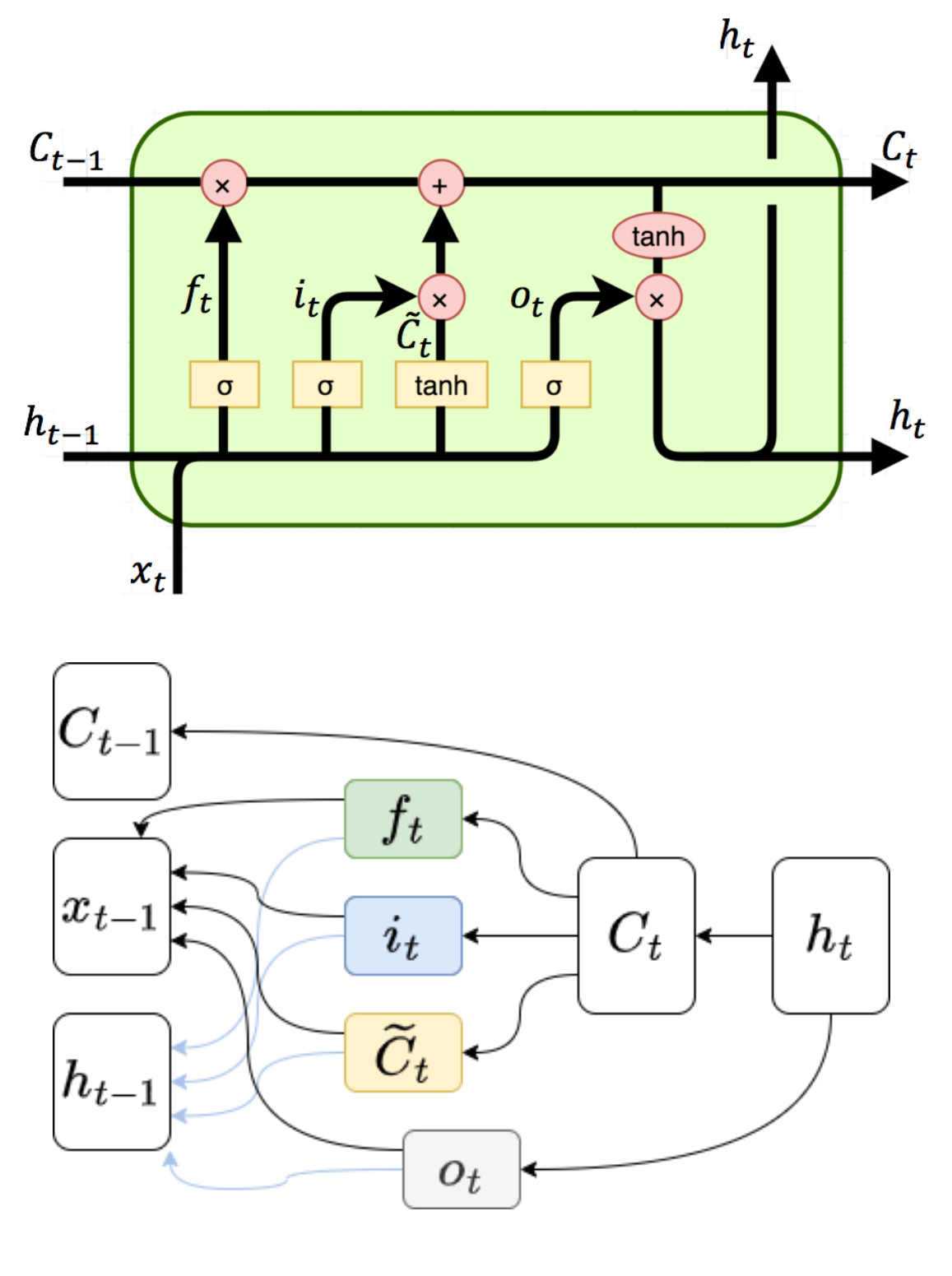
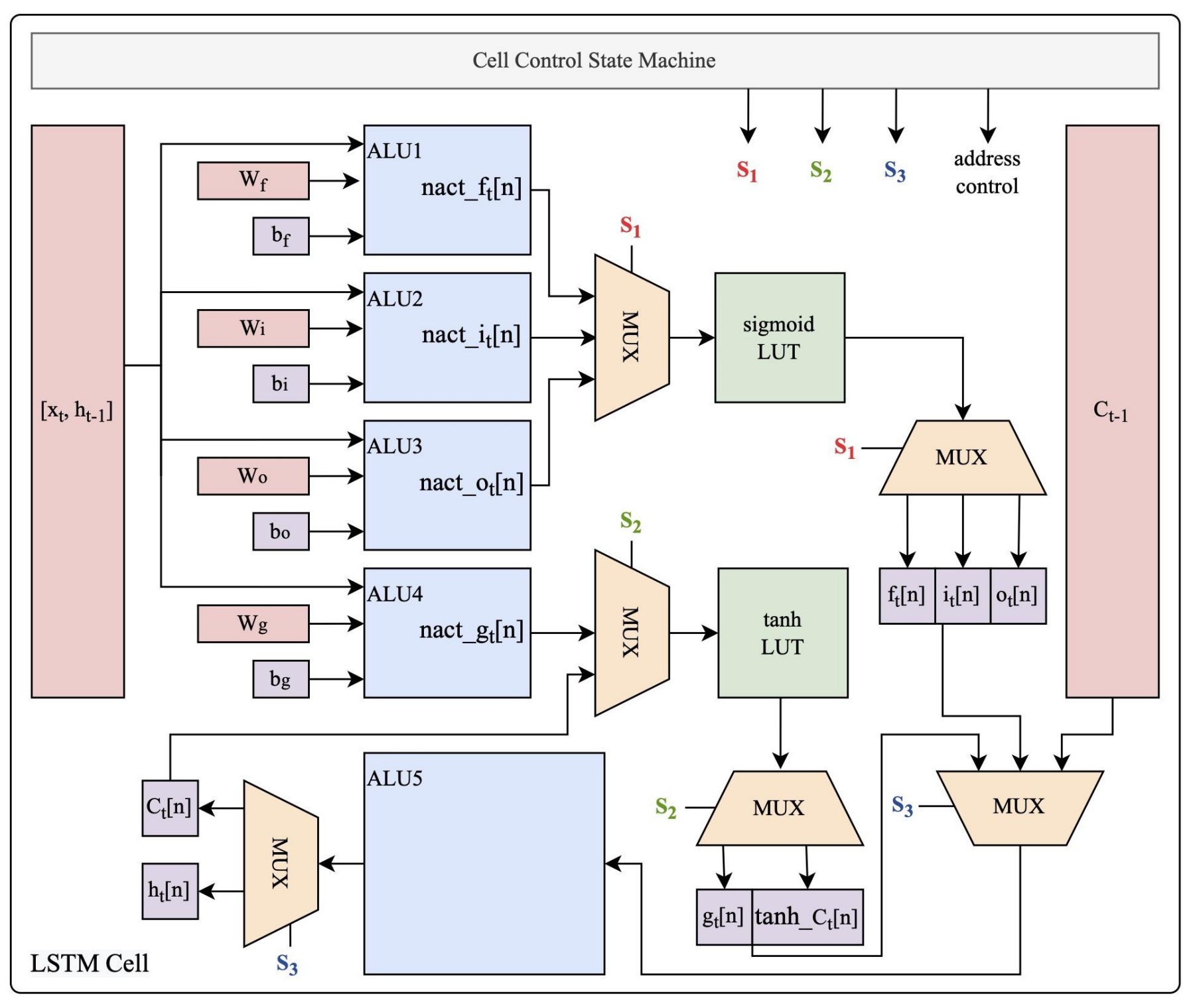
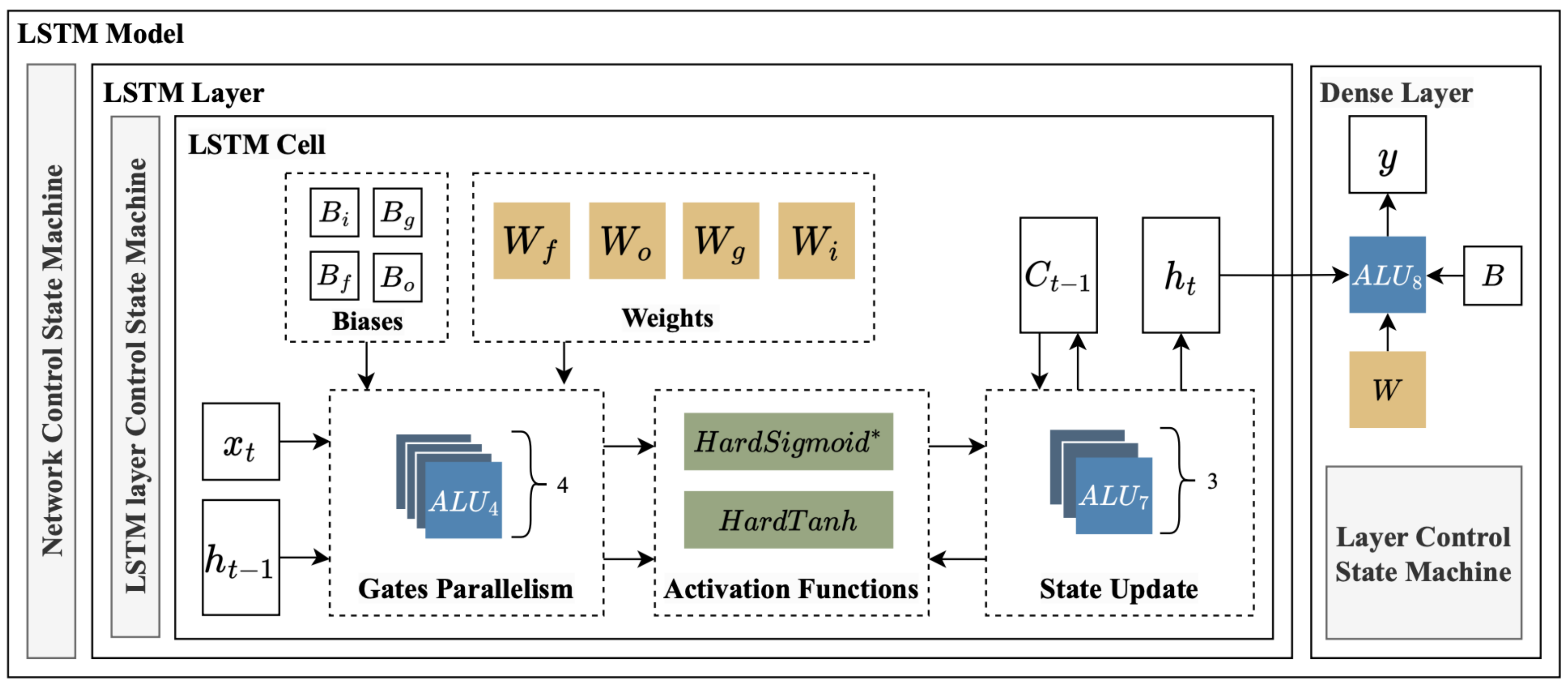


Illustration & Dependency Graph LSTM Cell



Improving Energy Efficiency by Gates Parallelization in LSTM Cell [1]



Improving Clock Frequency with Pipeline, Activation Functions Optimization [2] and Parameterization for Scalability and Stability [3]

AI Workload Awareness

FPGA operates in Duty-Cycle mode

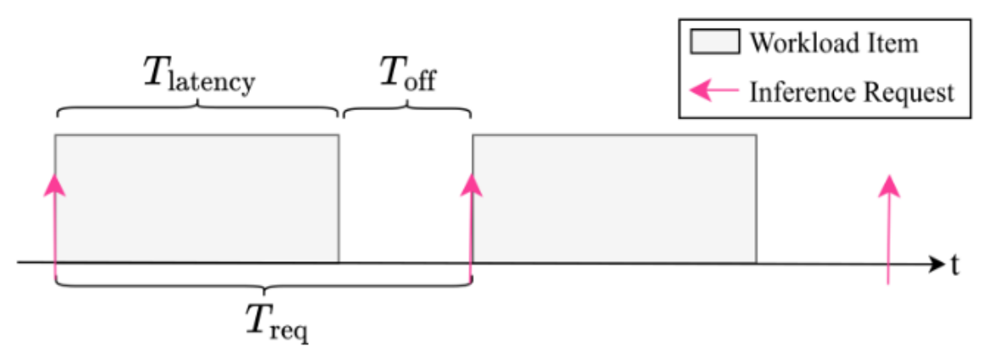
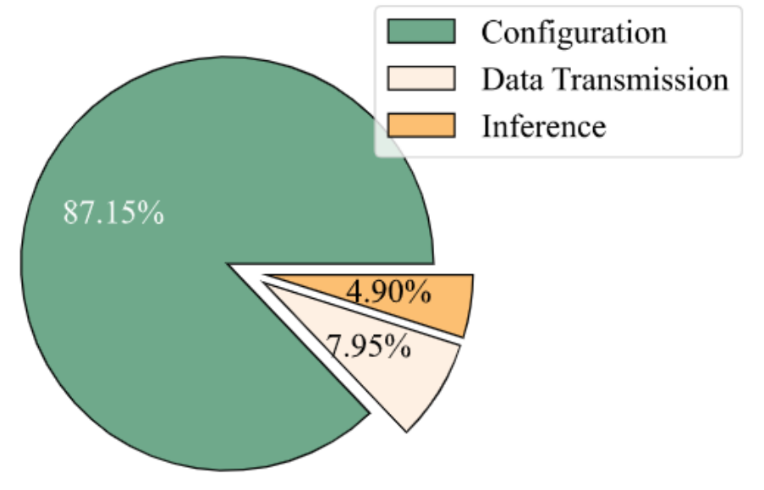


Illustration of On-Off Strategy [5]

But configuration overhead is …



Energy Breakdown of A Workload Item [4]

Our Approach: Idle-waiting Strategy

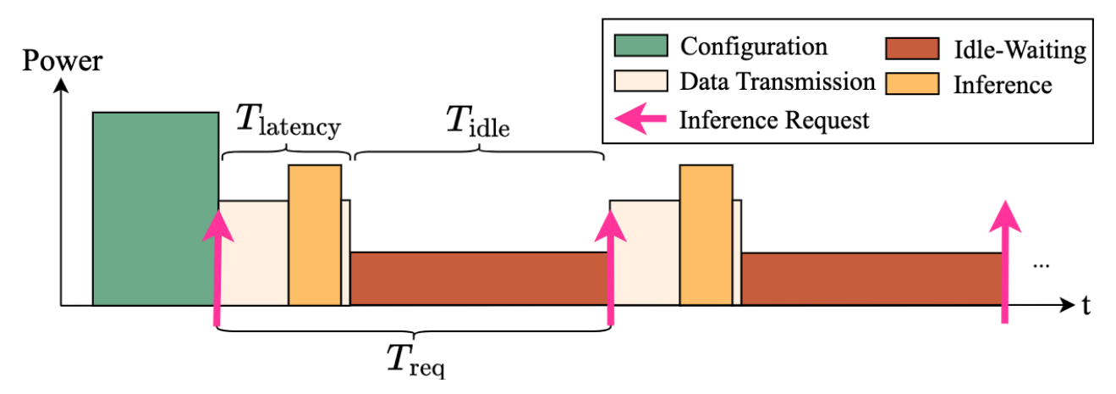
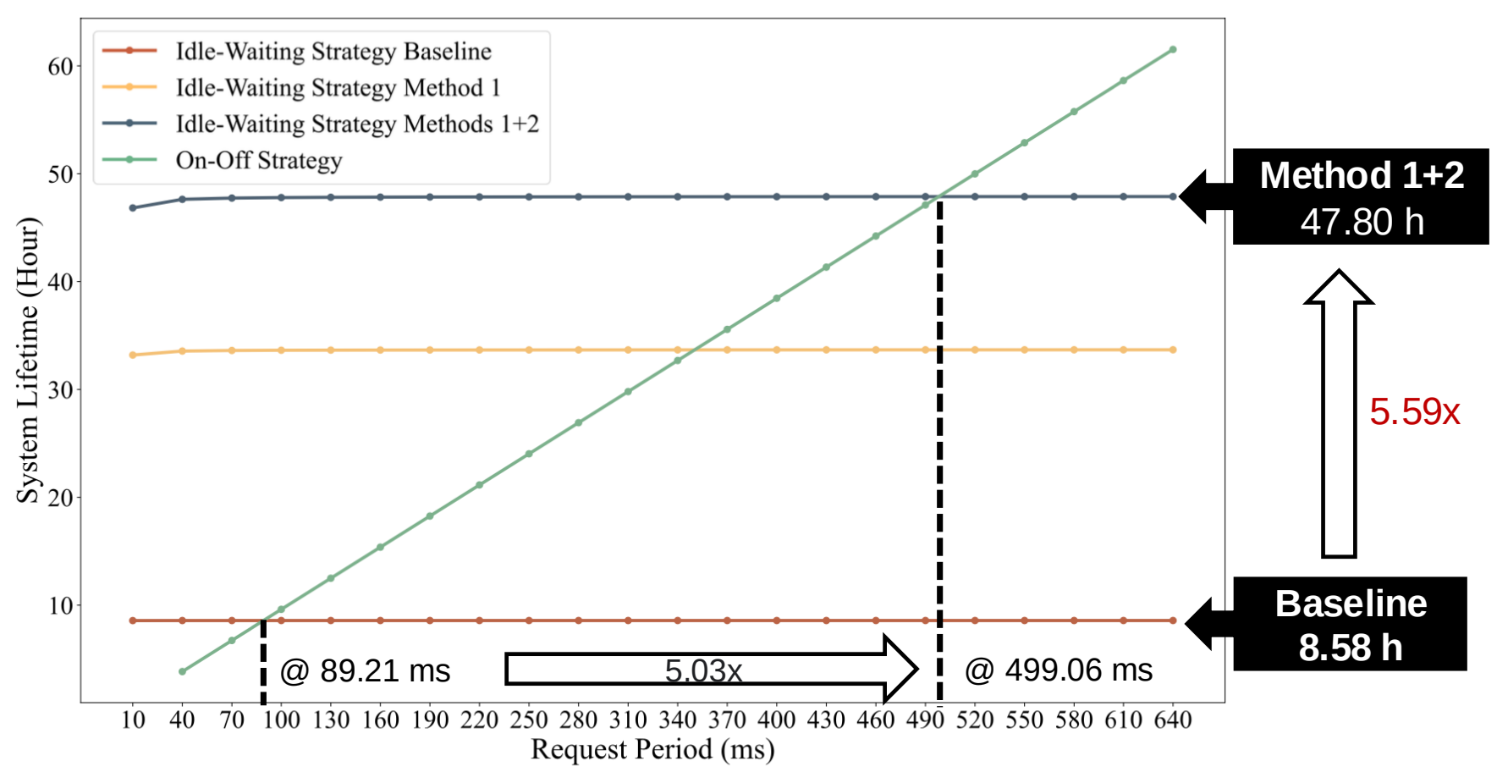


Illustration of Idle-Waiting strategy [5]



Baseline vs. Optimized Methods Across Request Periods [5]

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[2] Qian, Chao, Tianheng Ling, and Gregor Schiele. "Energy efficient LSTM accelerators for embedded FPGAs through parameterised architecture design." International Conference on Architecture of Computing Systems. 2023.

[3] Qian, Chao, Tianheng Ling, and Gregor Schiele. "Exploring energy efficiency of LSTM accelerators: A parameterized architecture design for embedded FPGAs." Journal of Systems Architecture 152 (2024): 103181.

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Knowledge Transferring

Concepts

- Design methodology: VHDL templates
- Optimizations: Pipeline, precomputation, parameterization
- Evaluation methodology: Software estimation + hardware validation

Architectures

- CNN accelerator for EEG Analysis [6]
- MLP for Flow estimation [7] [8]
- Transformer accelerator for Air Quality forecasting [9]

Elastic AI-Creator Toolchain for automation

- Providing optimized RTL templates for components of DL models [10]
- Eliminating the need for expertise in FPGA functionality for DL developers

ElasticAI-Creator
Toolchain
Scan Me!

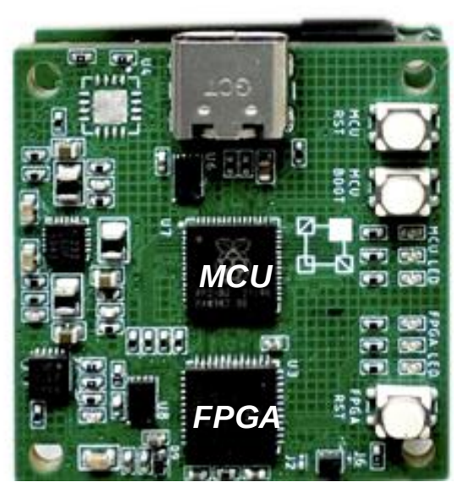
ElasticNode DL Acceleration Platforms

ElasticNode V5 [10]

- Dimension: 57.8 x 34 mm
- Cortex-M0+ MCU: RP2040
- Spartan-7 FPGA: S15, 25, S50
- SRAM(8Mb) + Flash(128Mb)
- Energy Meter: PAC1934
- Battery: 320mAh
- Extensions: ESP32, Sensors

ElasticNode V5 SE [12]

- Dimension: 34 x 34 mm
- ICE40UP5K
- Flash(16Mb)



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