



**Free and
Open Source
Silicon is
here to stay!**

**Philipp Wagner
FPGA Ignite Summer School
August 5, 2024**

**What's your
crazy idea?**

Untitled-1 X

1 *Select a language, or fill with template, or open a different editor to get started.
Start typing to dismiss or don't show this again.*



Our agenda

- How open source can help your crazy idea come true.
- How to do open source right.
- How the FOSSi Foundation can help.

About Philipp



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@imphil on GitHub

@MrImphil on Twitter

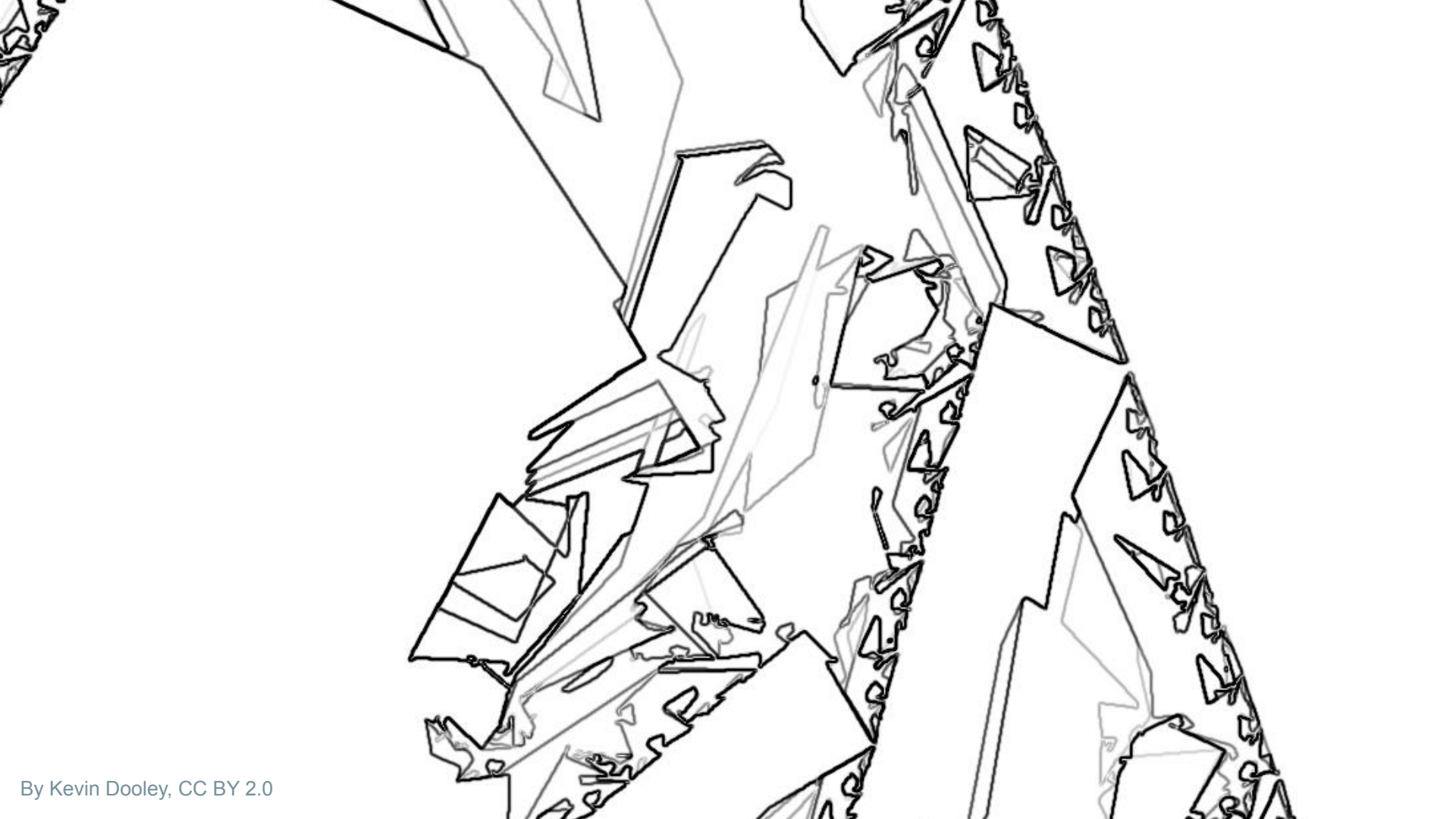
Defining Free and Open Source: The four fundamental freedoms

- The freedom to **run** the program as you wish, **for any purpose**.
- The freedom to **study** how the program works, and **change** it so it does your computing as you wish.
- The freedom to **redistribute** copies so you can help your neighbor.
- The freedom to **distribute copies of your modified versions** to others.

Free and Open Source licenses add color and legalese to these freedoms.



Interior view - Portland Art Museum - Portland, Oregon, USA., CC0



Building blocks

Frontend

Just like programming

“Programming languages”

High-Level Synthesis (HLS)

High-Level Languages

SystemVerilog and VHDL

Netlist

“All the other stuff”

Test Frameworks

Build tools

Developer productivity

Simulators

Hardware description

- (System)Verilog
- VHDL
- BlueSpec (Verilog/Haskell)
- Python-based
 - Migen
 - Amaranth HDL
 - MyHDL
- Based on functional programming languages
 - Spinal-HDL (Scala)
 - Chisel (Scala)
 - Clash (Haskell)
- **CIRCT: LLVM**

Reuse and integrate

- LiteX
- GitHub
- (OpenCores)
- ...

What can we do with a logic design?

- **Verify it**
- **Document it**
- **Make it look pretty**
- **Simulate it**
- **Run it on an FPGA**

Simulate it

GHDL

NVC



VERILATOR



Verification frameworks



SymbiYosys



Build and run

- FuseSoC and Edalize
- VUnit
- bazel_rules_hdl
- HDLMake
- ...

Developer productivity

- **Verible: lint, formatter, code indexer, language server, and more**
 - Formatting based mostly on the [lowRISC SV Style Guide](#)
- **Verilator lint**
- **VHDL Style Guide (VSG)**
- ...

Verilator lint

```
assign id_to_ping_d = (lfsr_state[PING_CNT_DW +: IdDw] >= NAlerts) ?  
                      lfsr_state[PING_CNT_DW +: IdDw] - NAlerts      :  
                      lfsr_state[PING_CNT_DW +: IdDw];
```

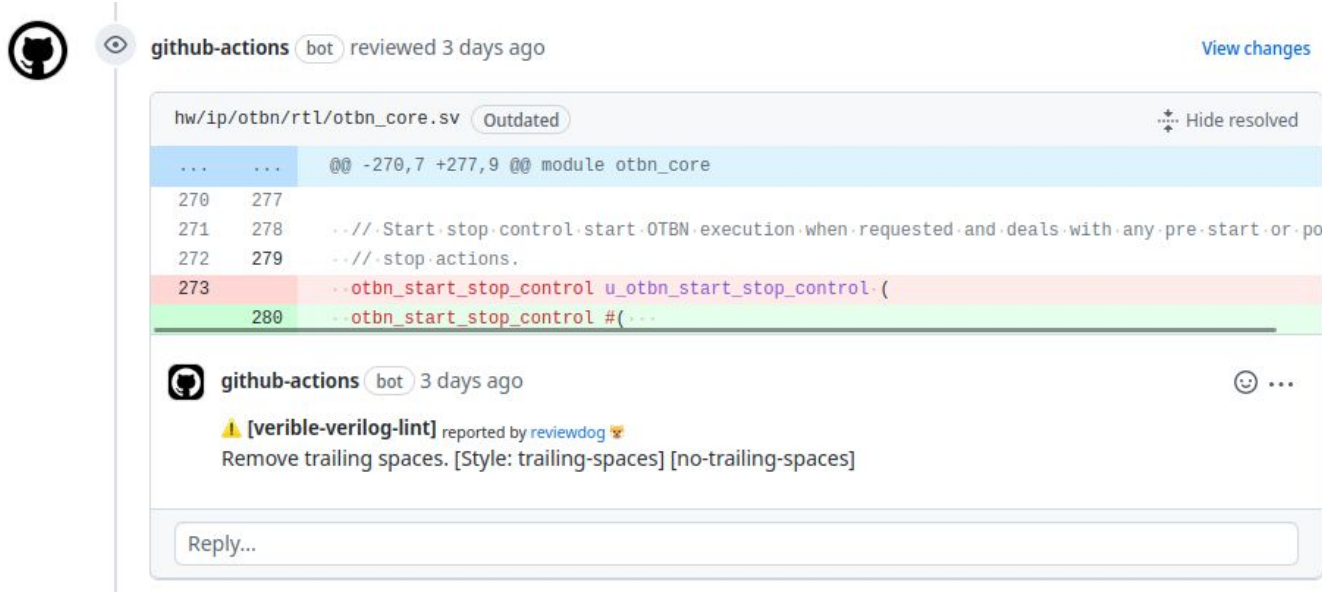
%Warning-WIDTH: ../src/lowrisc_ip_alert_handler_component_0.1/rtl/alert_handler_ping_timer.sv:131:58:
Operator GTE expects 32 bits on the LHS, but LHS's SEL generates 7 bits.

%Warning-WIDTH: ../src/lowrisc_ip_alert_handler_component_0.1/rtl/alert_handler_ping_timer.sv:132:57:
Operator SUB expects 32 bits on the LHS, but LHS's SEL generates 7 bits.

%Warning-WIDTH: ../src/lowrisc_ip_alert_handler_component_0.1/rtl/alert_handler_ping_timer.sv:131:70:
Operator COND expects 32 bits on the Conditional False, but Conditional False's SEL generates 7 bits.

%Warning-WIDTH: ../src/lowrisc_ip_alert_handler_component_0.1/rtl/alert_handler_ping_timer.sv:131:23:
Operator ASSIGNW expects 7 bits on the Assign RHS, but Assign RHS's COND generates 32 bits.

Automate reviews with Verible lint



The screenshot shows a GitHub pull request review. At the top, the reviewer is identified as 'github-actions bot' who reviewed 3 days ago. A 'View changes' link is visible. The code being reviewed is from the file 'hw/ip/otbn/rtl/otbn_core.sv' and is marked as 'Outdated'. The code snippet shows a Verilog module definition for 'otbn_core' with several lines of code. Line 273 is highlighted in red, indicating a lint error: '..otbn_start_stop_control u_otbn_start_stop_control. ('. Line 280 is highlighted in green, indicating a lint success: '..otbn_start_stop_control #(...'. Below the code, a comment from 'github-actions bot' 3 days ago reports the error: '[verible-verilog-lint] reported by reviewdog [no-trailing-spaces] Remove trailing spaces. [Style: trailing-spaces] [no-trailing-spaces]'. A 'Reply...' input field is at the bottom.

github-actions bot reviewed 3 days ago [View changes](#)

hw/ip/otbn/rtl/otbn_core.sv **Outdated** [Hide resolved](#)

```
... .. @@ -270,7 +277,9 @@ module otbn_core
270 277
271 278 ..// Start stop control start OTBN execution when requested and deals with any pre start or po
272 279 ..// stop actions.
273 ..otbn_start_stop_control u_otbn_start_stop_control. (
280 ..otbn_start_stop_control #(...
```

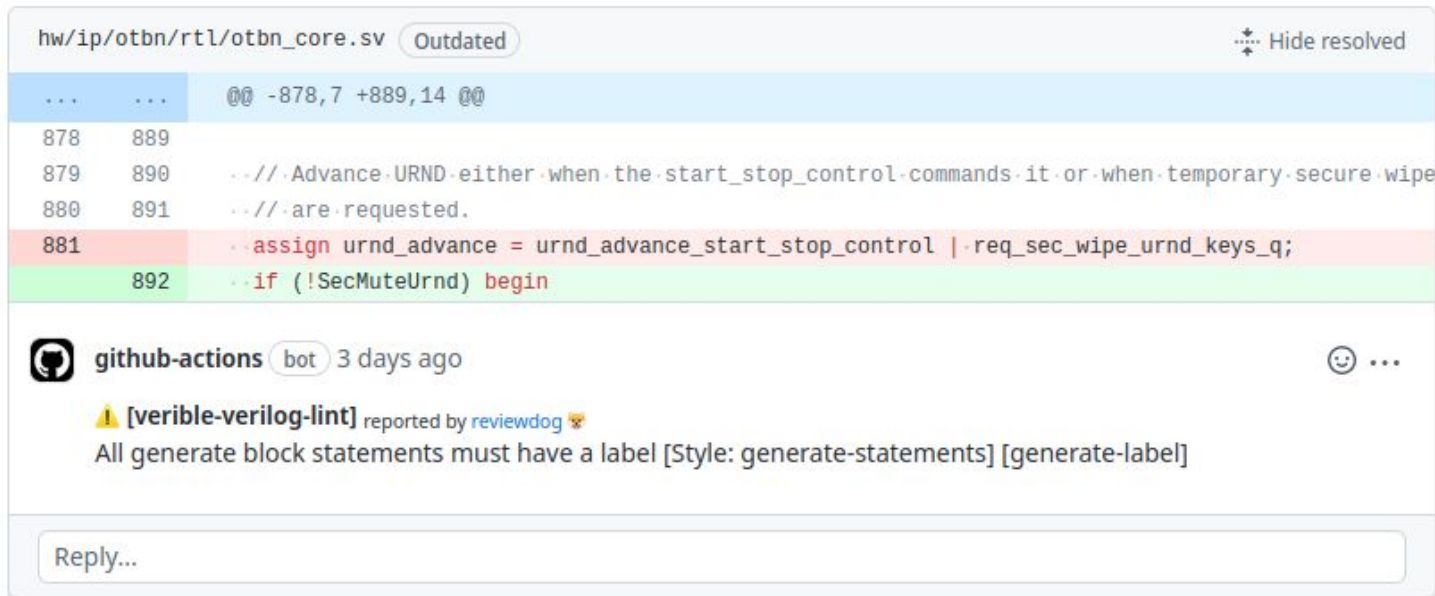
github-actions bot 3 days ago [...](#)

⚠ [verible-verilog-lint] reported by [reviewdog](#) 🐶
Remove trailing spaces. [Style: trailing-spaces] [no-trailing-spaces]

Reply...


Screenshot from <https://github.com/lowRISC/opentitan/pull/17195>

Automate reviews with Verible lint



The screenshot shows a GitHub pull request comment for the file `hw/ip/otbn/rtl/otbn_core.sv`, which is marked as `Outdated`. The comment includes a diff view of the code with a lint error highlighted in red. The error message is: `All generate block statements must have a label [Style: generate-statements] [generate-label]`. The code snippet shows an `assign` statement and an `if` block. The comment is from the `github-actions` bot, posted 3 days ago, and is reported by `reviewdog`.

```
hw/ip/otbn/rtl/otbn_core.sv Outdated ⚙ Hide resolved  
... .. @@ -878,7 +889,14 @@  
878 889  
879 890 ..// Advance URND either when the start_stop_control commands it or when temporary secure wipe  
880 891 ..// are requested.  
881 ..assign urnd_advance = urnd_advance_start_stop_control | req_sec_wipe_urnd_keys_q;  
892 ..if (!SecMuteUrnd) begin
```

 **github-actions** bot 3 days ago 😊 ...

⚠ [verible-verilog-lint] reported by reviewdog 🐕
All generate block statements must have a label [Style: generate-statements] [generate-label]

Reply...

Screenshot from <https://github.com/lowRISC/opentitan/pull/17195>

Summary

- The frontend is doing great.
- If we could only avoid re-inventing Verilog parsing.

Building blocks

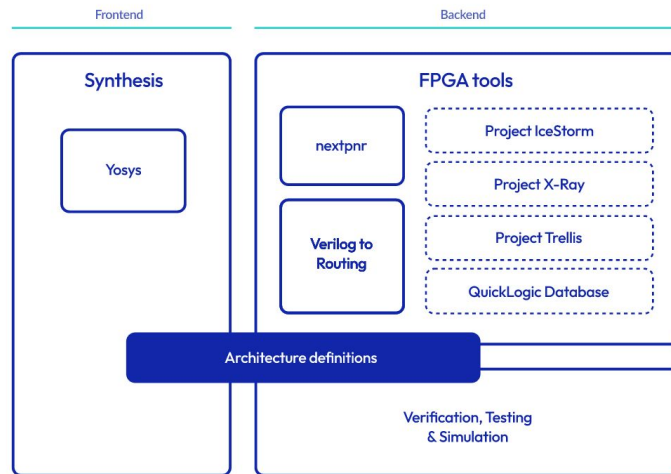
FPGA

Run it on an FPGA

F4FPGA (formerly SymbiFlow)



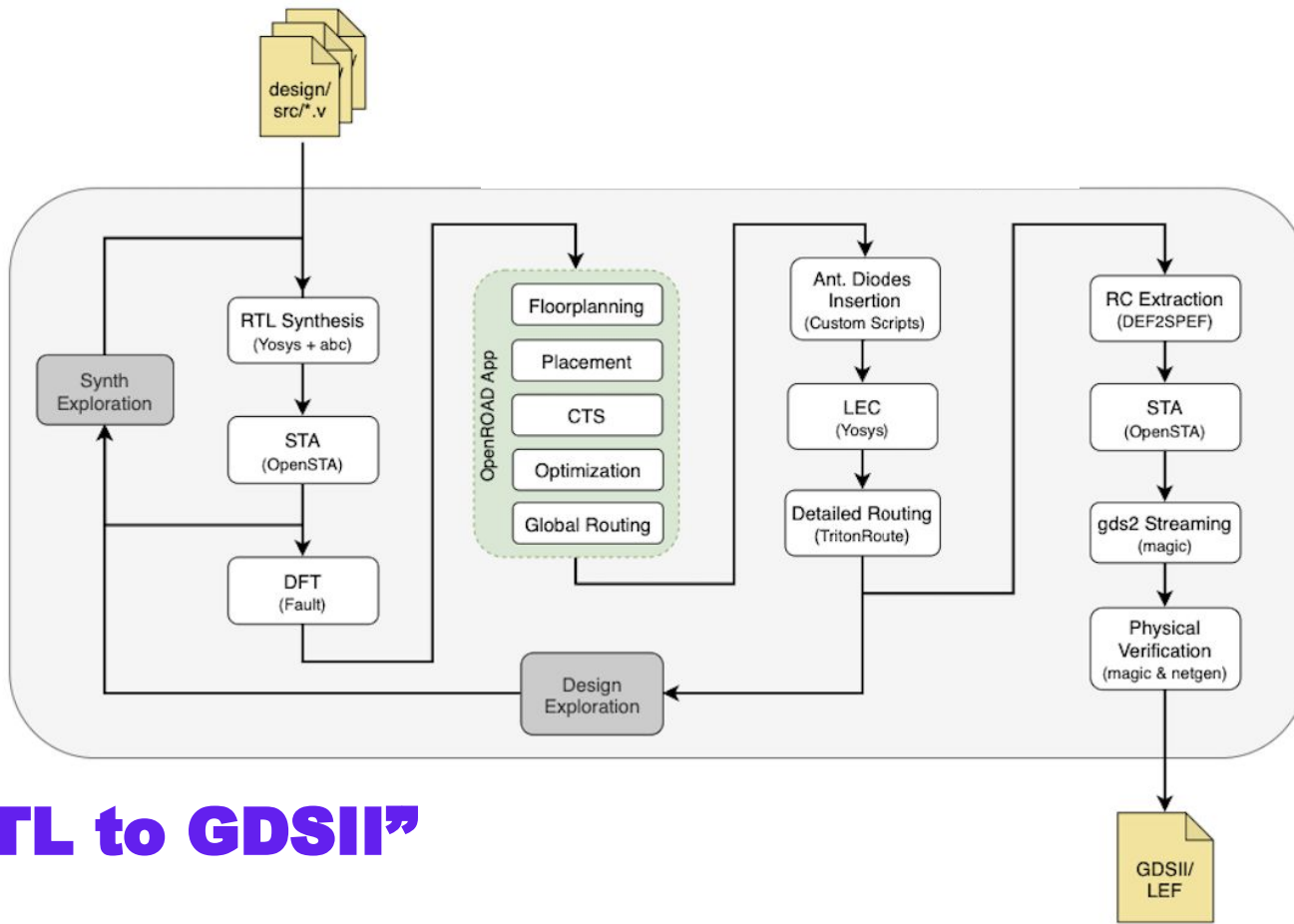
	Project Icestorm	Project Trellis	Project X-Ray	QuickLogic Database
Basic Tiles:	✓	✓	✓	✓
- Logic	✓	✓	✓	✓
- Block RAM	✓	✓	✗	✓
Advanced Tiles:	✓	✓	✗	✓
- DSP	✓	✓	✗	✓
- Hard Blocks	✓	✓	✗	✓
- Clock Tiles	✓	✓	✓	✓
- IO Tiles	✓	✓	✓	✓
Routing:	✓	✓	✓	✓
- Logic	✓	✓	✓	✓
- Clock	✓	✓	✓	✓



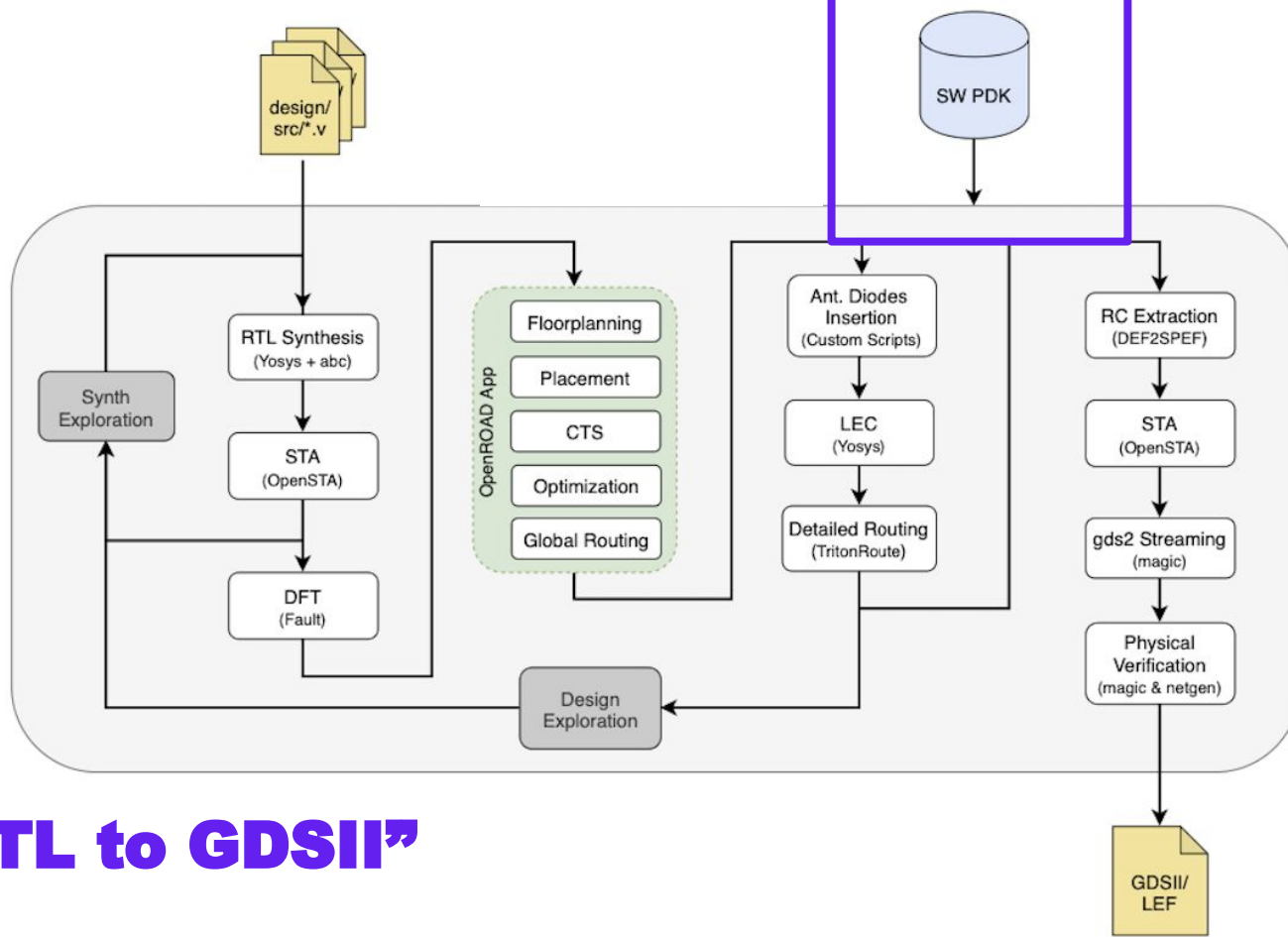


Building blocks

Backend



“RTL to GDSII”



“RTL to GDSII”

Building blocks

The Process Design Kit (PDK)

The video player displays a diagram on the left with a central red circle labeled 'ASIC'. Three green arrows point towards it from 'RTL Design' (top), 'EDA Tools' (left), and 'PDK Data' (right). A dashed green circle surrounds the central ASIC. To the right of the diagram, the text 'PDK Data' is shown above a play button icon and three red question marks '???'.

On the right side of the player, the FOSSI Foundation logo (a puzzle piece icon) is at the top, followed by the text 'FOSSI Foundation'. Below this is a video thumbnail of a man with a beard and glasses. At the bottom right of the player area, the text 'FOSSI Dial-Up' is visible.

Below the video player, the title reads: '[FOSSI Dial-Up] Tim Ansell - Skywater PDK: Fully open source manufacturable PDK for a 130nm process'. The channel name is 'FOSSI Foundation' with 3600 subscribers and an 'Abonnieren' button. Engagement icons show 649 likes, a share icon, 'Teilen', and 'Speichern'.

[FOSSI Dial-Up] Tim Ansell - Skywater PDK: Fully open source manufacturable PDK for a 130nm process

FOSSI Foundation
3600 Abonnenten
Abonnieren

649 | [Share icon] | Teilen | [Save icon] | Speichern | ...

28.443 Aufrufe vor 2 Jahren gestreamt

Screenshot from <https://www.youtube.com/watch?v=EcwW2IWdnOM>

June 2020

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Mit umfangreichem Software-Angebot

ALDI informiert

...ab Mittwoch, 26. März

Der MEDION Titanium MD 8008 mit Intel® Pentium® 4 Prozessor 2,6 GHz

Einmalig

Der neue ALDI-PCXL Titanium MD 8008 von MEDION

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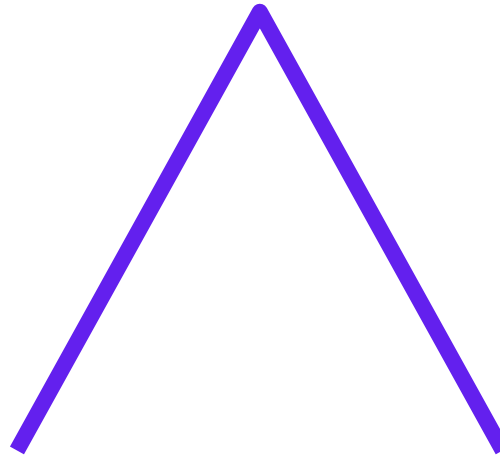
ALDI MARKT **ALDI SÜD**

- intel inside pentium 4
- ECHTE 2,6 GHz
- 512KB Second Level Cache • Motherboard mit 3PC-Steckplätzen • Grafik aufrüstbar durch AGP 8x Steckplatz • Arbeitsspeicher aufrüstbar durch einen freien Speichersteckplatz.
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Get most out of open source

**Open
Participation**

**Enable everyone
to contribute.**



**Allow everyone
to use and modify**

**Open
Source**

Open participation: your rewards

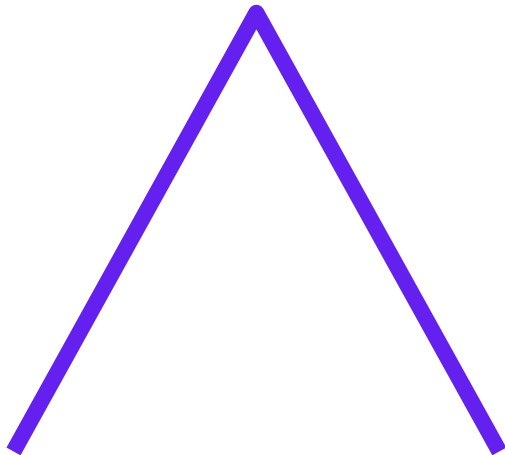
- **Attract contributors**
 - Code, docs, bug reports, testing, ports
- **Attract users**
 - Project activity is a major (perceived) quality indicator
- **Accessible and transparent “support channels” are important**
 - Help your business or group at university
 - If everyone can join easily, new hires or PhD candidates can as well.
 - Peer-to-peer help

Open participation

```
assign open_participation =  
    (internal_dev == outside_contributor);
```


How do we get there?

**Open
Participation**



Open Source

- + Open communication
 - + Build and test infrastructure
 - + Tool access (reproducibility)
 - + Documentation (design, process)
 - + Clear licensing
- All code, tests, scripts

The FOSSi Foundation

About FOSSi Foundation

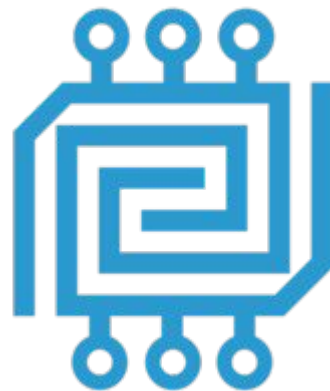
The FOSSi Foundation exists to **promote and protect the open source silicon chip movement**. It actively encourages the community's growth and is helping to maintain the open spirit of the movement, through **events, educational programmes and working groups**. With an international membership of experts from academia and industry, it **supports new open source initiatives and collaborations** – offering free advice to governments and policy makers, corporations, academics and hobbyists. As a **not-for-profit organisation**, the foundation is independent of any commercial interests and acts as a steward in support of open source projects which broadly benefit the open source silicon community. FOSSi is an acronym for Free and Open Source Silicon.

Join the community!



By Andrzej Otrębski, CC BY-SA 3.0

ORConf 2024

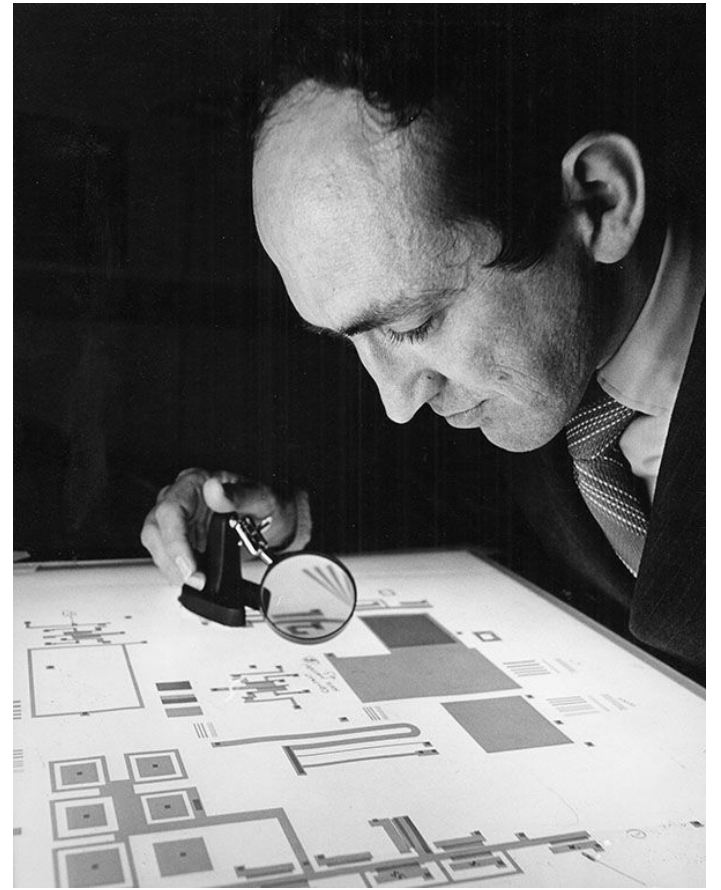


**September 13 - 15, 2024
Goteborg, Sweden**

<https://fossi-foundation.org/orconf/2024>

**“There’s an end to
scaling.**

**But there’s no end
to creativity.”**



Robert H. Dennard

There's no end to creativity

- **Unpredictable innovation.**
- **Simpler, more accessible, better tools.**
- **Democratized access! (part of it: cost)**
- **Revolutionize learning!**

An atmosphere of excitement and anticipation pervades this field. Workers from many backgrounds, computer scientists, electrical engineers, and physicists, are collaborating on a common problem area which has not yet become classical. The territory is vast, and largely unexplored. The rewards are great for those who simply press forward.

C. Mead and L. Conway, Introduction to VLSI systems. Addison-Wesley
Reading, MA, 1978.



**Free and Open
Source Silicon
is a reality
today.**

Join the fun!